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Technical Committee

AAL1 Circuit Emulation Over Packet Switched Networks

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1. Introduction

At the present time, much of the carrier “voice-over-packet” traffic is transported over ATM networks using the AAL1 adaptation layer. As carriers consider packet switched networks or PSN (e.g. IP,MPLS, etc.), which are not based on ATM, it makes good sense to consider the suitability of using principles based upon AAL1 to support circuit emulation services without an underlying ATM layer. AAL1 is a mature, well-understood technology that has been successfully deployed. Reusing AAL1 technology for circuit emulation over packet networks provides a proven method for the communications industry to deliver carrier grade and carrier scale circuit emulation services.

This document describes an AAL1-based circuit emulation scheme suitable for non-ATM networks. No technical changes are proposed to the core AAL1 operation itself (including timing recovery).

2. Reference Architecture

The reference model for the transport of TDM over PSN (TDMoPSN) is shown in Figure 2.1. It consists of the following elements:

- Packet-switched core, consisting of routers or switches (e.g., Label Switching Routers).
- Provider Edge (PE) devices providing network interworking functions between the TDM and packet networks.
- TDM devices connected to a framed or unframed TDM Interface via Attached Circuits (AC). The AC can be a TDM link or extended over another network, such as ATM.

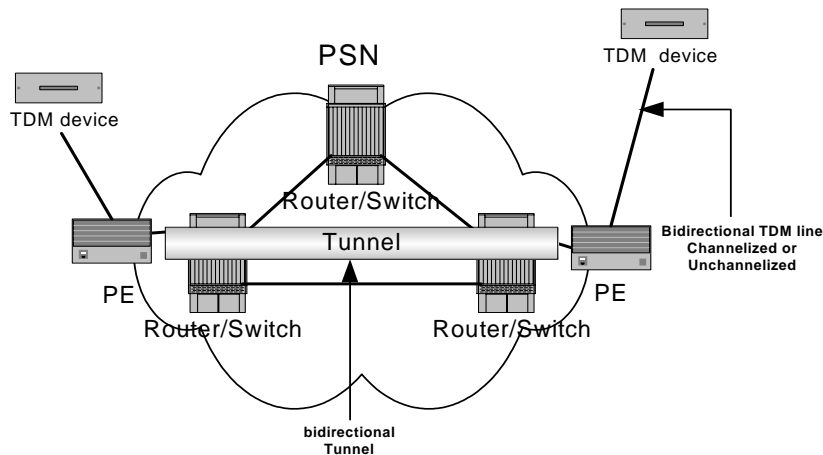


Figure 2-1 TDM over PSN Network Reference Architecture.

A PSN network connects two TDM networks. The TDM service is first provisioned or signaled between the TDM interface of the PE device and the TDM device. A bi-directional tunnel (e.g., LSP) is then created either by manual provisioning or by using a signaling protocol (e.g., CR-LDP, RSVP-TE) to carry the pseudo-wire (PW), which in turn is provisioned or signaled to carry the circuit emulation connection. The use of the packet network by two TDM networks and/or devices is not visible to the end users. The PE provides all mapping and encapsulation functions necessary to ensure that the service provided to the TDM networks and/or devices is unchanged by the presence of a PSN. In this document, the ingress direction refers to data flow into the PSN (from a TDM or ATM network). The egress direction refers to data flow out of the PSN (into a TDM or ATM network).

3. TDM over PSN Interworking Requirements

This section lists the requirements to be met for the transport of TDM over PSN.

TDM transport: Must support transfer of TDM traffic: framed (including fractional/channelized) and unframed T1/E1, n x 64kbps, and T3/E3 over PSN.

Frame Ordering: Must preserve frame ordering end-to-end.

Signaling transport: Must provide for transparent transfer of CAS signaling.

Timing: May provide a mechanism for reconstruction of the TDM clock per ANSI/T1.101-1999 [25] or appropriate ITU-T G.810, G.823 and G.824 recommendations [6,7,8].

Alarm transport: Must support the transport of standard alarms to and from the TDM interface across the PSN network.

Alarm mapping: Must support the mapping of PSN faults / alarms to the TDM interface.

Interworking: Must interwork with existing AAL1 services without requiring processing of AAL1 encapsulation.

Overhead vs. latency trade-off: Must have the option to configure, either manually or by a signaling protocol, the number of AAL1 cells per frame, in order to balance between overhead and latency.

3.1 TDM Services

Table 1 describes supported TDM services.

Table 1. TDMoPSN Services.

Service	Type	Standard	Rate
Synchronous serial	Unstructured	V.35,V.36,V.37	-----
T1	Unstructured	G.703 [3]	1.544Mbps
E1	Unstructured	G.703 [3]	2.048Mbps
E3	Unstructured	G.751 [5]	34.368Mbps
T3	Unstructured	T1.107 [2]	44.736Mbps
N * 64K	Structured	I.231 [26]	N x 64kbps
E1	Structured	G.704 [4]	1.984 Mbps (see Note 2)
Fractional E1	Structured	G.704 [4]	n x 64Kbps 1 <= n <=31
T1	Structured	G.704 [4]	1.536 Mbps (see Note 2)
Fractional T1	Structured	T1.107 [2]	n x 64Kbps, n x 56Kbps 1 <= n <=23
Channelized / Fractional T1 with CAS	Structured	G.704 [4], T1.107 [2]	n x 64 Kbps, n x 56 Kbps 1 <= n <= 23
Channelized / Fractional E1 with CAS	Structured	G.704 [4]	n x 64 Kbps, 1 <= n <= 30
AAAL-1	Unstructured , Structured (see Note 1)	ITU-T I.363.1 [11], af-vtoa-0078.000 (1997) [9]	All of the above

- Both data and clock information must be transferred edge to edge.
- When present, CAS signaling is transparently transferred edge to edge.
- Trunk-associated CCS signaling is transparently transferred edge to edge.
- Standard TDM alarms are generated when required and transferred edge to edge.

Note 1: When AAL1 uses the partial cell fill option as described in af-vtoa-0078.000 [9] Section 2.2.2 and ITU-T Recommendation I.363.1 [11] Section 2.5.2.5, removal of the dummy or fill octets prior to interworking with the PSN to conserve bandwidth in the packet network is for further study.

Note 2: For structured T1 and E1 services, the data rate does not include framing overhead.

3.2 PSN Quality of Service

TDMoPSN does not provide a mechanism to ensure timely packet delivery nor provide other quality of service guarantee; these functions are left to the PSN.

TDMoPSN assumes a network with prioritization and sufficient bandwidth, low probability of bit error, packet misordering or lost packets.

Switches and routers through which the TDMoPSN stream must traverse, should be configured to respect packet priorities. If Diffserv is used to provide QoS, then EF-PHB should be used with proper conditioning at the ingress PE. Sufficient bandwidth can be guaranteed by under-subscription and/or traffic engineering.

4. TDM over PSN Encapsulation

4.1 Layering Model

The protocol-layering model for TDM over PSN is shown in Figure 4.1, where higher layers appear lower in the diagram.

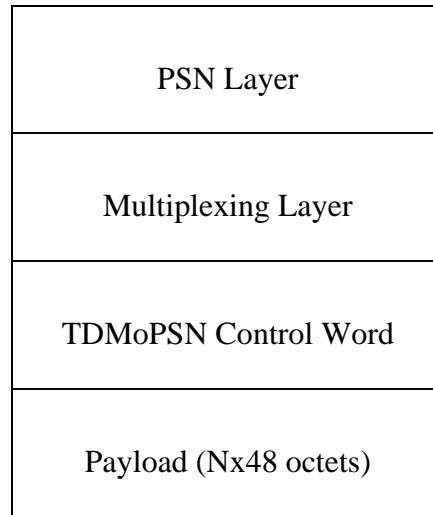


Figure 4-1 TDM over PSN Packet Encapsulation.

The TDMoPSN Encapsulation header shall contain the TDMoPSN Control Word (4 bytes) and may also contain optional timing information. If the optional timing information is included in the TDMoPSN header, it shall immediately precede the TDMoPSN control word in case of an IPv4 or IPv6 PSN, and shall immediately follow it in the case of an MPLS PSN or Ethernet PSN (see Fig. 4.2 and Fig. 4.3 below). A pseudo-wire consists of a multiplexing layer, TDMoPSN control word and (optional) timing information.

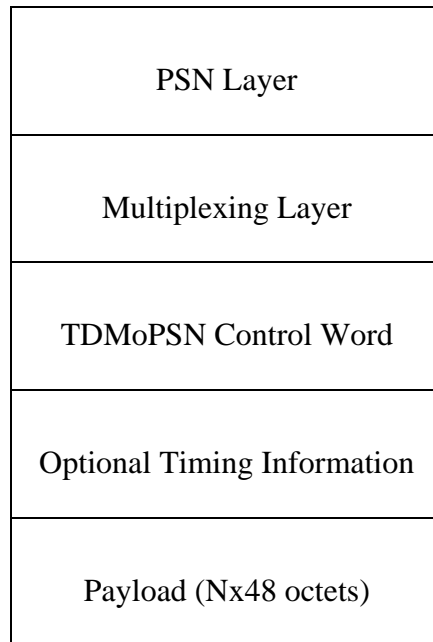


Figure 4-2 TDM over Non-IP (e.g., MPLS/Ethernet) Encapsulation.

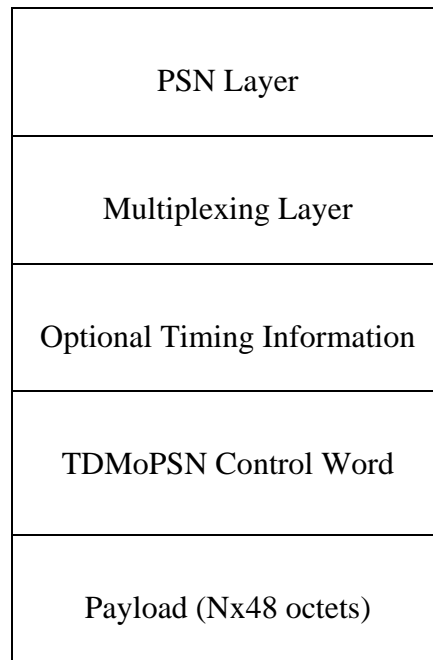


Figure 4-3 TDM over IP PSN (IPv4/IPv6) Encapsulation.

4.2 PSN Layer

The PSN layer covers all packet-based infrastructures, such as IP, MPLS, or Ethernet. The PSN is assumed to be reliable enough and of sufficient bandwidth to enable transport of the required TDM data. Due to the general applicability of this specification to various PSN protocols, the terms “packets” and “frames” are used interchangeably in this document.

4.3 Multiplexing Layer

Edge devices may handle more than one circuit bundle at a time. A circuit bundle is defined as an AAL1-framed stream of bits that have originated from a single physical interface or from interfaces that share a common clock, which are transmitted from a single TDMoPSN source device to a single TDMoPSN destination device. For example, bundles may comprise some number of 64 Kbps timeslots originating from a single E1, or an entire T3 or E3. Circuit bundles are uni-directional streams, but are universally coupled with bundles in the opposite direction to form a bi-directional connection. The multiplexing layer is responsible for multiplexing multiple circuit bundles into the same PSN tunnel.

If a TDMoPSN edge device is required to handle multiple circuit bundles, then it is the responsibility of the multiplexing layer to provide a circuit bundle identifier (CBID) in order to enable differentiation between these circuits. Examples of multiplexing layers include MPLS, UDP, L2TPv3 and GRE.

Each pseudo-wire can carry only one circuit bundle. A tunnel can carry multiple pseudo-wires. The multiplexing layer is used to multiplex several pseudo-wires in the same tunnel; it uses the CBID to differentiate between its constituent pseudo-wires.

4.4 Optional Timing Information

Optional timing information may be carried using the RTP header defined in sub-clause 5.1 of [10].

If the RTP header is present, then for IPv4 and IPv6 PSNs, the RTP header shall appear immediately before the control word of each interworking packet. Otherwise, the RTP header shall appear in each interworking packet immediately after the control word and immediately before the payload. The fields of the RTP header shall be encoded as follows:

V (version) is always set to 2.

P (padding), X (header extension), CC (CSRC count) and M (marker) are always set to 0. RTP header extensions, padding and contributing synchronization sources are never used.

PT (payload type) is encoded as follows:

- A PT value shall be allocated from the range of dynamic values for each direction of the interworking tunnel.
- The ingress IWF shall set the PT field in the RTP header to the allocated value.

The sequence number in the RTP header shall be equal to the sequence number in the control word.

Timestamps are used for carrying timing information over the network. Their values are generated in accordance with the rules established in [10].

The clock frequency used for generating timestamps shall be an integer multiple of 8 kHz.

The SSRC (synchronization source) field in the RTP header may be used for detection of misconnections.

4.5 TDMoPSN Control Word

The 32-bit control word must appear in every TDMoPSN packet. Its format is given in the following figure.

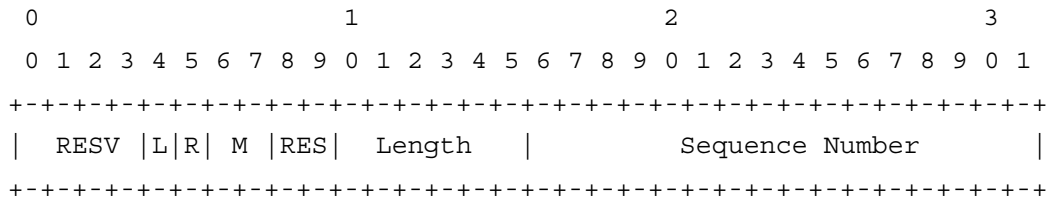


Figure 4-4 TDMoPSN Control Word.

Table 2. TDMoPSN Control Word Fields

Field	Meaning
Bits 0-3: Reserved	Reserved bits. Set to zero on transmission and ignored on reception.
Bit 4: L bit	The L bit is used together with the M bits (6 and 7) to indicate various fault conditions. See section 5.2 for encoding details.
Bit 5: R bit	When set to 1, it indicates that the egress PE is not receiving packets at its TDMoPSN receive port.
Bits 6-7: M bits	The M bits are used in combination with the L bit to indicate various conditions (see section 5.2 for encoding details).
Bits 8-9: Reserved	Reserved bits. Set to zero on transmission and ignored on reception.
Bits 10-15: Length	The length field is used to indicate the use of padding to meet minimum transmission length requirements of the layer 2 network. It shall be used if the TDMoPSN packet length (including layer 2 overhead) is less than 64 bytes, and shall be set to zero if this length is equal to or exceeds 64 bytes.
Bits 16-31: Sequence number	The 16-bit sequence number can be used to detect lost packets and packet mis-ordering . Generation (on transmission) and processing (upon reception) of the sequence number field is mandatory.

4.6 TDMoPSN Payload

The AAL1 protocol is a natural choice for trunking applications. Although originally developed to adapt various types of application data to the rigid format of ATM, the mechanisms are general solutions to the problem of transporting constant or variable bandwidth data streams over byte-oriented packet networks. For the prevalent case in which timeslot allocation is static and no activity detection is performed, the payload can be most efficiently encoded using constant bit rate AAL1 adaptation. The AAL1 format is described in ITU-T standard I.363.1 [11]; its use for TDM circuit emulation is explained in ATM Forum specification af-vtoa-0078.000 [9]).

The TDMoPSN payload consists of one or more 48-octet sub-frames, whose maximum value is determined by the maximum frame size of the layer 2 network or target latency constraints set by the network operator. The number of sub-frames, which can be inferred by the receiving side from the total length of the payload, is pre-configured and typically chosen according to latency and bandwidth constraints. Using a single sub-frame reduces latency to a minimum, but incurs the highest overhead, while using, for example, eight sub-frames reduces the overhead percentage while increasing the latency by a factor of eight.

An implementation shall support one sub-frame per frame. It should support more than one sub-frame per frame.

Some multiple-access network architectures have overhead characteristics that impose a limit on the number of frames that can be sent in a given time. In these cases, it may be necessary to support more than one sub-frame per PSN frame for proper operation.

The interworking method proposed in this document can also be used for structured AAL1 CES with partial cell fill to reduce SAR PDU payload assembly delay (at the expense of reduced bandwidth efficiency across the PSN). When AAL1 uses the partial cell fill option as described in af-vtoa-0078.000 [9] Section 2.2.2 and ITU-T Recommendation I.363.1 [11] Section 2.5.2.5, removal of the dummy or fill octets prior to interworking with the PSN to conserve bandwidth in the packet network is for further study.

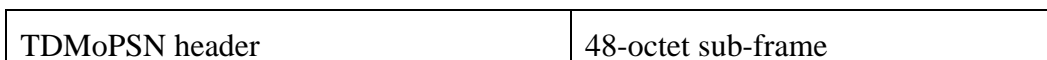


Figure 4-5 Single TDMoPSN AAL1 sub-frame per TDMoPSN frame.

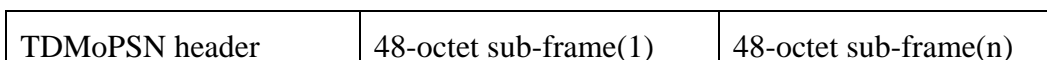


Figure 4-6 Multiple TDMoPSN AAL1 sub-frames per TDMoPSN frame.

The first octet of each 48-octet AAL1 sub-frame is an AAL1 control word, whose format is shown below.

Bit 0	Bit 1-3	Bits 4-6	Bit 7	
C	SN	CRC	P	47 octets of payload

The constituent bits of the first octet are defined as follows:

C (1 bit): Convergence sub layer indication. Its use here is limited to indication of the existence of a pointer (see below). C=1 if a pointer is present. C=0 otherwise.

SN (3 bits): Sequence Number. Increments from sub-frame to sub-frame.

CRC (3 bits): Cyclic Redundancy Check code over C and SN

P (1 bit): even-bit Parity

For TDM network interworking, the egress PE could use the integrity check available at the Layer 2 frame that encapsulates the sub-frames, and therefore would not normally check the contents of the CRC and P bits in the AAL1 cell header. On the other hand, for ATM service interworking in the ingress direction, the CRC and P bits of the AAL1 sub frame needs to be checked at the egress PE, since the sub-frame had originated from an ATM network that is being terminated. Consequently, the CRC and P bits in an AAL1 subframe shall be checked, since the egress PE may not be aware of which interworking mode is being used.

The structure of the remaining 47 octets in the TDMoPSN AAL1 sub-frame depends on the sub-frame type, of which there are three, corresponding to the three types of AAL1 circuit emulation service defined in ATM forum specification [9]. These are known as unstructured circuit emulation, structured circuit emulation and structured circuit emulation with CAS.

5. TDMoPSN Fault Management

5.1 Fault Handling

PSN fault handling consists of fault indication, detection and mapping, as described in the following subsections.

5.1.1 PSN Fault Detection and Mapping

PSN CES faults can be detected by using several PSN OAM mechanisms related to different PSN technologies. This document does not mandate the use of any specific OAM mechanism. The sequence number in the control world may also be used to detect PSN faults. The PE must be able to suppress IWF alarms that result from PSN faults.

TDMoPSN UP or DOWN states refer to the ability to forward traffic over both directions. The TDMoPSN CES should be considered down even if only one direction of the PSN CES is down.

When a PSN tunnel-down condition is detected, notification of the fault is propagated across the PSN towards the IWF.

The IWF will map the fault to the appropriate AC fault as specified in section 5.3.

PSN fault detection is discussed in Appendix A.

5.1.2 Fault Indication

This document uses L, R and M bits in the control word in order to convey fault state information as described in the following section.

5.2 Alarm Indication

R bit

When set to 1, the R-bit indicates that the egress IWF is not receiving packets at its TDMoPSN receiving port. This indication is important as it reflects the state of the PSN tunnel. This bit is equivalent to PSN RDI (if available on the specific PSN OAM).

L and M bits

The L and M bits are used as follows:

L	M	
0	00	indicates no local defect
0	10	reserved
0	10	reports a far-end TDM RAI condition.
1	11	reserved.
1	00	indicates a local defect. When interworking with TDM networks, it indicates a local trunk failure (e.g., LOS, OOF) or a TDM layer failure (e.g., TDM AIS). When interworking with ATM networks, it indicates an ATM layer failure (e.g., F4/F5 AIS) or physical layer failure.
1	01	reserved.
1	10	reserved.
1	11	reserved.

5.3 Alarm and Failure Handling

This section discusses the general principles and requirements for alarm and failure handling. It is based mainly on the same principles used in the ATM Forum's CES 2.0 specification [9]. ATM CES alarm and failure handling are shown in this section for analogy only.

Appendix C describes the various modes of operation that apply to circuit emulation over PSN. The remainder of this section describes failure-handling for these modes. The figures use solid arrows to indicate "shall" or "should" behavior and dashed arrows to indicate either "may" or an alternative behavior.

Appendix B.1 contains further details and state diagrams regarding behavior under applicable defect conditions; it is provided for information only.

5.3.1 Trunk Conditioning for Structure-Aware Trail-Terminated Emulation over PSN

This mode is normally used when it is not desirable to indicate the failure at one of the local TDM networks to the far-end TDM network.

5.3.1.1 Trunk Conditioning for LOS, OOF, AIS

This section describes how the IWF should behave in case of detection of Loss of Signal (LOS) or Out Of Frame synchronization (OOF), or reception of TDM AIS at the TDM interface of an IWF.

ATM CES 2.0 requires generating trunk conditioning in the downstream direction and generating RDI in the upstream direction as shown in Figure 5-1.

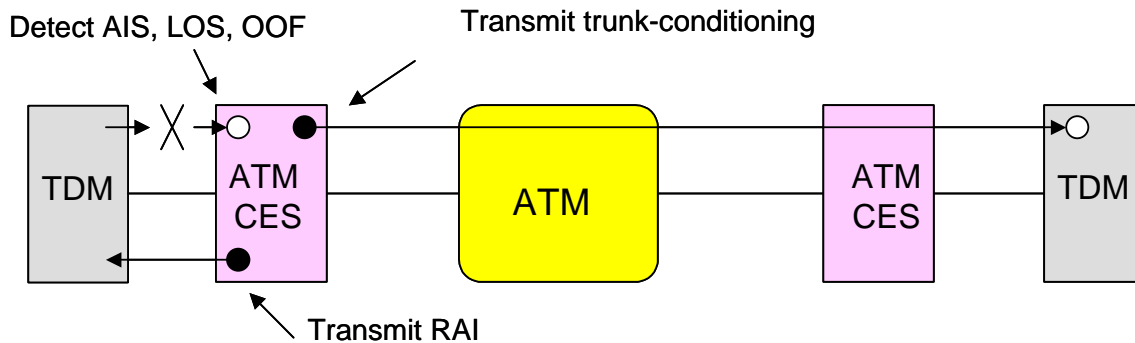


Figure 5-1 ATM CES 2.0, Ingress TDM failure handling (Structured).

Similar requirements can be applied to the PSN CES.

Rule1: When LOS, OOF or AIS is detected at the TDM interface of an IWF, the PSN CES IWF shall: Apply Trunk Conditioning in the downstream direction, or alternatively, set L=1 and M=00, and send packets downstream with either no payload or with a dummy payload. Procedures for Trunk Conditioning are described in Bellcore TR-NWT-000170 Issue 2, Section 2.5 [24]. A Remote Alarm Indication (RAI, or ‘yellow’) shall always be delivered in the upstream direction.

Rule 2: Upon reception of packets with L=1 and M=00, the IWF shall ignore the payload and apply Trunk Conditioning in the downstream direction. Procedures for Trunk Conditioning are described in [24].

These rules are shown in Figure 5-2.

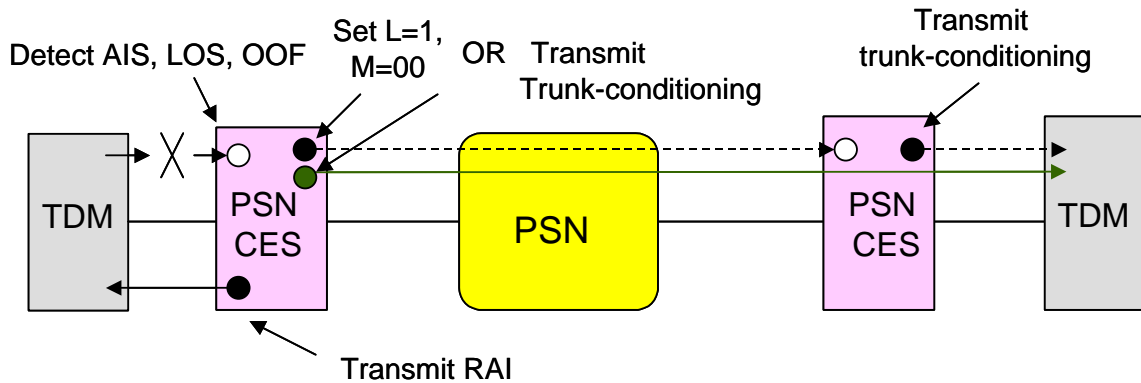


Figure 5-2 PSN CES, TDM failure handling (Structure-Aware Trail-Terminated).

5.3.1.2 Trunk Conditioning for Packet Loss or Buffer Starvation

This section describes how the IWF should behave in case of detection of packet loss or buffer starvation at the PSN interface of an IWF.

ATM CES 2.0 requires generating trunk conditioning in both the downstream and upstream directions, as shown in Figure 5-3.

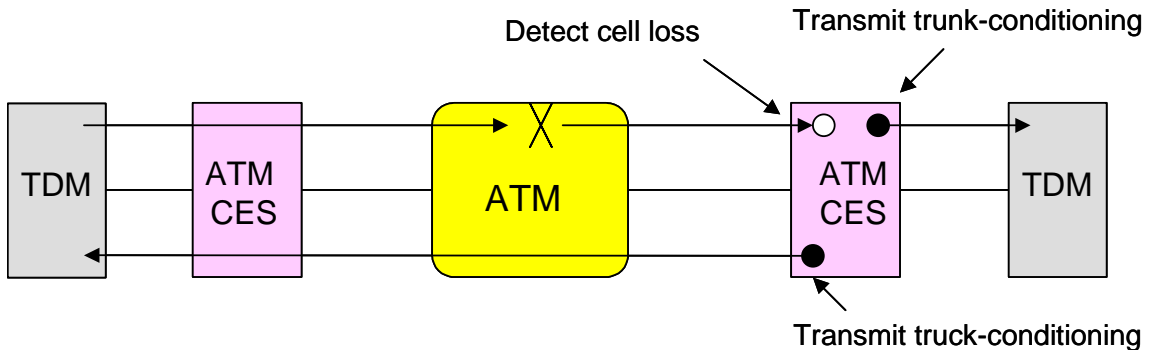


Figure 5-3 ATM CES 2.0, Cell Loss/Buffer Starvation handling (Structured).

Similar requirements can be applied to the PSN CES.

Rule 3: After an integration period, a persistent packet loss or buffer starvation condition detected at the PSN CES IWF shall trigger Trunk Conditioning in the downstream direction, as specified in [24]. It should also set the R-bit to 1 in the upstream direction. It may additionally send Trunk Conditioning upstream.

This requirement is shown in Figure 5-4.

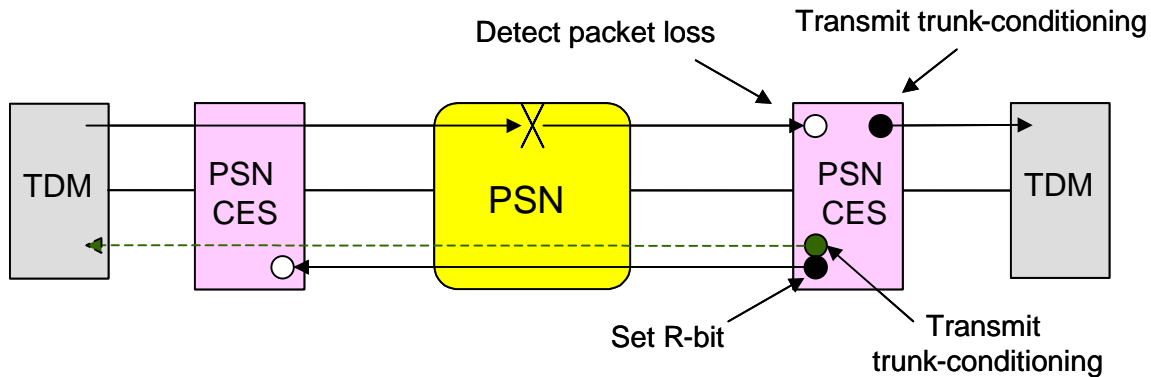


Figure 5-4 PSN CES, Packet Loss/Buffer Starvation handling (Structure-Aware Trail-Terminated).

Rule 4: Any TDM RAI signal received at the TDM interface of a PSN CES IWF shall be terminated.

5.3.2 Trunk Conditioning for Structure-Agnostic Emulation over PSN

This mode is typically used to transport the bit stream without knowing its underlying structure.

5.3.2.1 Trunk Conditioning for LOS

This section describes how the IWF should behave when LOS is detected at the TDM interface of an IWF.

ATM CES 2.0 requires that TDM AIS be generated in the downstream direction. Furthermore, all alarms, including the RAI generated by the far-end TDM equipment in response to AIS, should pass through the ATM network transparently. This is shown in Figure 5-5.

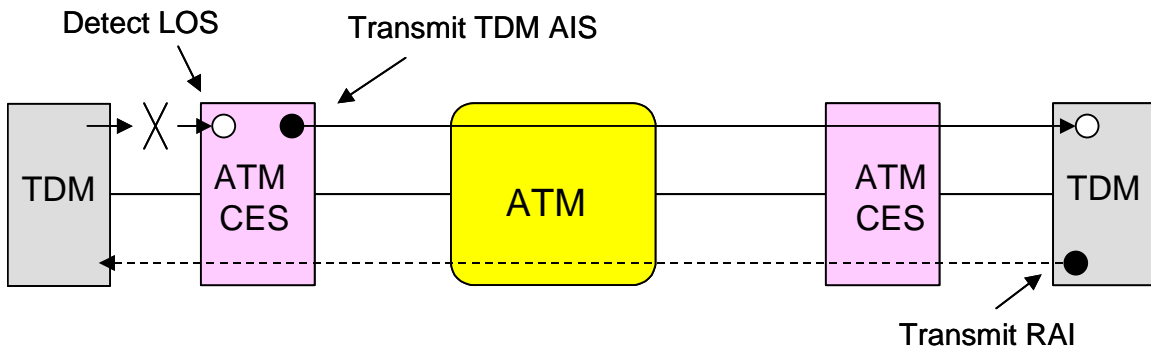


Figure 5-5 ATM CES 2.0, TDM failure handling (Unstructured).

Similar requirements can be applied to the PSN CES.

Rule 5: When LOS is detected at the ingress TDM interface, the PSN CES IWF shall: generate TDM AIS in the downstream direction, or alternatively, send packets with L set to 1 and M set to 00 without a payload or with a dummy payload in the downstream direction.

Rule 6: Upon receiving packets with L=1 and M=00, an IWF shall ignore the payload and generate TDM AIS toward the TDM network.

These rules are shown in Figure 5-6.

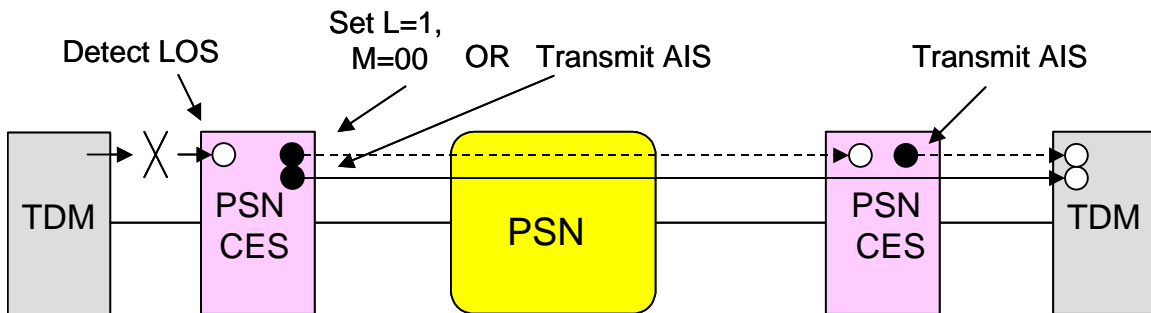


Figure 5-6 PSN CES, TDM failure handling (Structure-Agnostic).

5.3.2.2 Trunk Conditioning for Packet Loss or Buffer Starvation

This section describes how the IWF should behave if buffer starvation or persistent packet loss is detected at the egress CES IWF. ATM CES 2.0 [9] requires that TDM AIS be generated in the downstream direction, as shown in Figure 5-7.

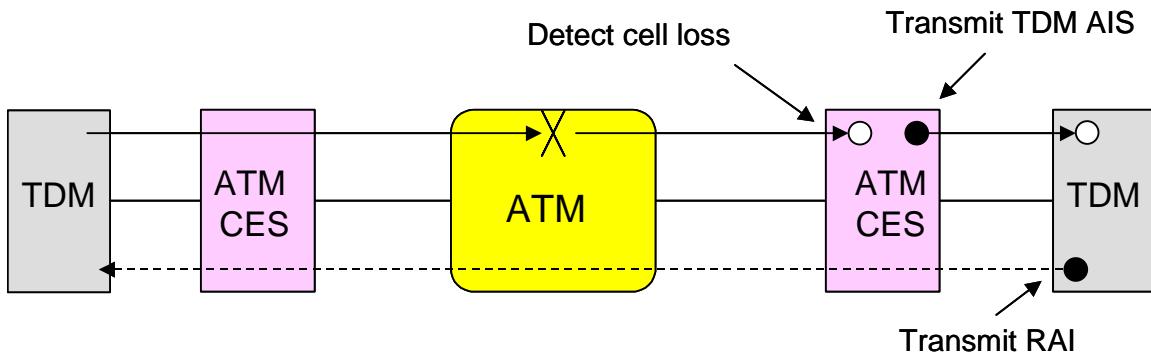


Figure 5-7 ATM CES 2.0, Cell Loss/Buffer Starvation handling (Unstructured).

A similar requirement can be applied to the PSN CES.

Rule 7: After an integration period, a persistent packet loss or buffer starvation condition detected at the PSN CES IWF shall trigger TDM AIS generation in the downstream direction. It should also set the R-bit to 1 in the upstream direction.

This requirement is shown in Figure 5-8.

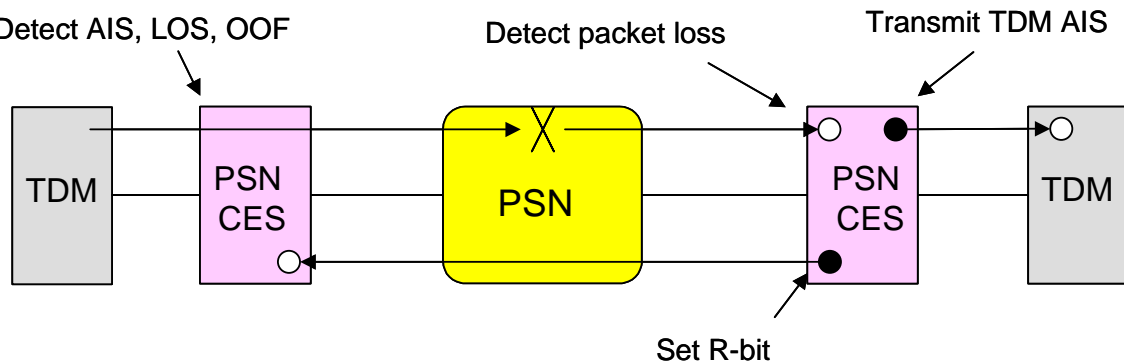


Figure 5-8 PSN CES, Packet Loss/Buffer Starvation Handling (Structure-Agnostic).

5.3.2.3 Handling of TDM RAI

Rule 8: TDM RAI received at the input of the service interface is carried through to the output service interface without modification. This rule is shown in Figure 5-9.

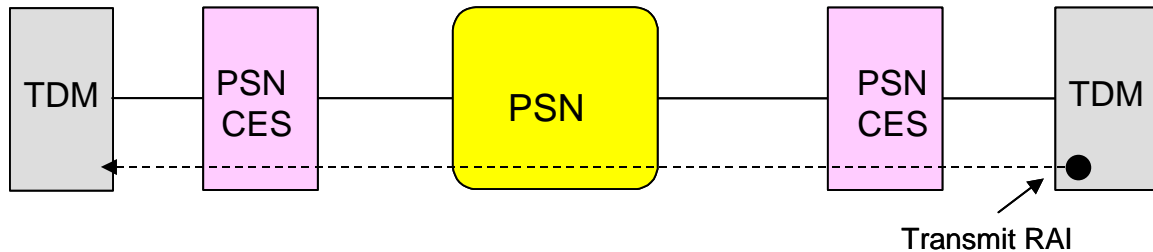


Figure 5-9 TDM RAI Handling (Structure-Agnostic).

5.3.3 Trunk Conditioning for Structure-Aware Trail-Extended Emulation over PSN

This mode is normally used when it is desirable to indicate failure at one of local the TDM networks to the far-end TDM network. This mode has no equivalent in ATM CES 2.0 [9].

5.3.3.1 Trunk Conditioning for LOS, OOF and AIS

This section describes how the IWF should behave in case of detection of LOS or OOF or reception of TDM AIS at the TDM interface of an IWF.

Rule 9: When LOS, OOF or TDM AIS is detected at the TDM interface, the PSN CES IWF shall transmit packets with no payload or with dummy payload in the downstream direction. It must set the L and M flags of these packets to L=1 & M=00.

Rule 10: Upon reception of packets with L=1 & M=00, the IWF shall ignore the payload and send TDM AIS downstream.

These rules are shown in Figure 5-10.

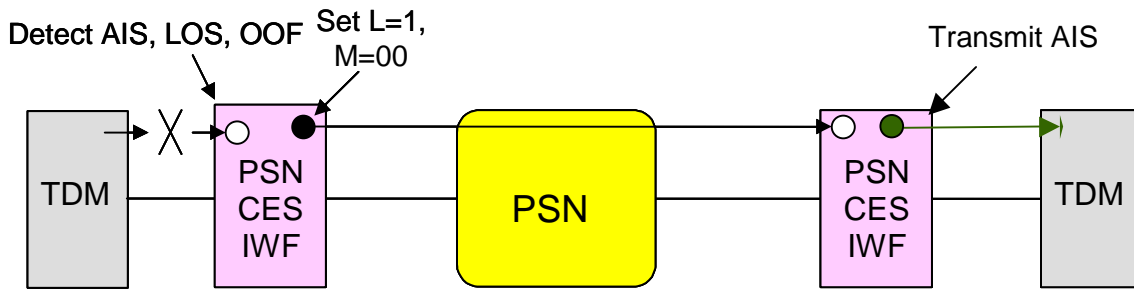


Figure 5-10 PSN CES TDM Failure Handling (Structure-Aware Trail-Extended Mode).

5.3.3.2 Trunk Conditioning for Packet Loss or Buffer Starvation

This section describes how the IWF should behave upon detecting buffer starvation or persistent packet loss at its PSN interface.

Rule 11: If the IWF detects a persistent packet loss or buffer starvation condition during an integration period, it shall generate AIS in the downstream direction. It should also set the R-bit to 1 in the upstream direction. This requirement is shown in Figure 5-11.

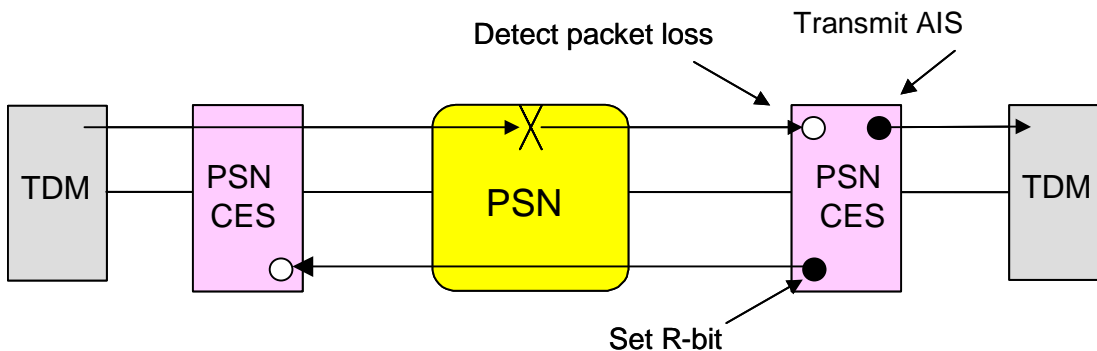


Figure 5-11 PSN CES Handling of Packet Loss or Buffer Starvation (Structure-Aware Trail-Extended Mode).

5.3.3.3 Handling of TDM RAI

Rule 12: When TDM RAI is received at the TDM interface of an IWF, the IWF shall clear the L bit to 0 and set the M bits to 10.

Rule 13: Upon reception of packets with L=0 and M=10, the IWF shall send TDM RAI on its TDM interface.

These rules are shown in Figure 5-12.

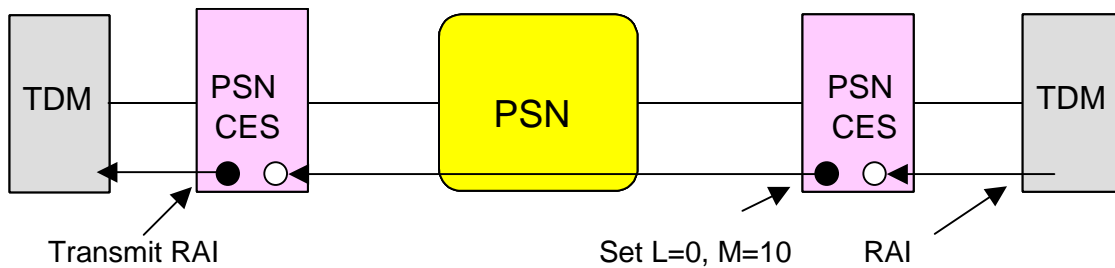


Figure 5-12 TDM RAI Handling (Structure-Aware Trail-Extended Mode).

6. TDMoPSN Frame Processing

6.1 Generating TDMoPSN Frames

The process of constructing a TDMoPSN frame consists of generating AAL1 (48-byte) PDUs, aggregating several of these PDUs into one packet, and adding control, multiplexing and PSN headers.

6.2 Generating the TDMoPSN Payload

AAL1 PDUs are generated as specified in [9] and [11]. The number of PDUs per packet is as configured by the system.

6.3 Generating the TDMoPSN Control Word

6.3.1 Setting the Sequence Number

The 16-bit sequence number is defined separately for each Circuit Bundle (CB). It may be used by the receiver to detect lost or out-of-order packets. In addition, since the basic clock rate for each CB is constant, the sequence number may be used as an approximate timestamp for synchronization purposes.

The following procedure shall be used by the ingress IWF:

- For security purposes, the sequence number shall be set to a pseudo-random value for the first packet transmitted on the PW associated with the TDMoPSN service.
- For each TDMoPSN frame sent over a given PW, the corresponding CB's sequence number shall be incremented by 1, modulo 2^{16} .
- When RTP is used, its sequence number shall be identical to the sequence number in the control word.

6.3.2 Generating the L, M and R bits

The following procedure shall be used by the ingress IWF in a given TDMoPSN service:

Set L=1, M=00

When a TDM AIS, OOF or LOS is detected at the TDM interface of the PSN CES IWF. This response is mandatory in structure-aware trail-extended mode only. It is an alternative response optional in structure-aware trail-terminated and in structure-agnostic modes.

Set L=0, M=10

When TDM RAI is detected at the TDM interface of a PSN CES IWF. This response applies only to structure-aware trail-extended mode.

Set L=0, M=00

When none of the defects listed above are detected.

All Other Combinations of L and M:

Are reserved for future use.

Set R=1

When persistent packet loss is detected at the PSN interface of the PSN CES IWF. This response is recommended but not mandatory. Persistent packet loss is defined as no packets received for a preconfigured interval. The default value of this interval is 1 second.

Set R=0

When persistent packet loss is not detected.

6.3.3 Setting the Length Field

The Length field provides, in units of octets, the size of the TDMoPSN frame payload, whose value is the sum of:

- a. size of the control word (4 octets),
- b. size of the optional timing information, and
- c. size of the payload (total of all of the constituent sub-frames);

If this sum equals or exceeds 64 octets, the Length field shall be set to zero.

6.4 Generating the Multiplexing Header

The multiplexing header is generated and CBID is set according to which circuit bundle to which the AAL1 PDUs belong. Each multiplexing technology may use different fields to encode the CBID. For example, if the multiplexing header is MPLS, then the MPLS label (20 bits) is used as the CBID. For UDP and L2TPv3, the source port number or session ID could be used, respectively, to encode the CBID.

6.5 Generating the Optional RTP Header

An RTP header is optionally generated according to [10]. The RTP sequence number must match the sequence number of the TDMoPSN control word.

The fields of RTP header shall be used as follows:

V (version) is always set to 2

P (padding), X (header extension), CC (CSRC count) and M (marker) are always set to 0. Accordingly, RTP header extensions, padding and contributing synchronization sources are never used.

PT (payload type):

- A PT value shall be allocated from the range of dynamic values for each direction of the PW.
- The ingress IWF shall set the PT field in the RTP header to its allocated value.

Timestamps are used for carrying timing information over the network:

- Their values are generated in accordance with the rules established in [10].
- The clock frequency used for generating timestamps should be an integer multiple of 8 kHz.

The SSRC (synchronization source) field in the RTP header may be used for detection of misconnections.

6.6 Generating the PSN Header

The PSN header is generated according to the underlying PSN protocol architecture. The PSN header fields must be set to values that ensure delivery of the TDMoPSN frame to the correct egress PE (e.g., appropriate IP destination address, MAC destination address, or MPLS label).

6.7 Receiving TDMoPSN Frames

When a PE receives a TDMoPSN frame, it checks the layer 2 checksum; if the checksum is incorrect, the frame is discarded. Otherwise, it processes the TDMoPSN frame header fields and AAL1 PDUs, as described in [11] and [9], in order to restore the TDM traffic for transmission through one of its TDM interfaces. The PE also performs the following actions (not necessarily in the order shown):

- The PE processes the length and sequence number fields.
- It also processes the AAL1 header fields of each constituent PDU (sub-frame) and extracts TDM traffic that is then sent towards the TDM interface.
- The receiver checks the CRC, P and SN bits in the AAL1 PDU.
- When a frame is received from the PW associated with the TDMoPSN service, its sequence number must be processed as follows:

- The expected sequence number is considered to be unknown until the first packet has been received from the PSN network.
- The first packet received from the PSN network is always considered "in order"; the expected sequence number is set to the value contained in that first packet.
- If the received sequence number is equal to or greater than the expected sequence number in a cyclic sense [27], then the frame's content is placed into the playout buffer, and the expected sequence number is set to the received number incremented by 1 modulo 2^{16} .
- Otherwise, the received frame is dropped and the expected sequence number is left unchanged.

When frames have been lost, the appropriate amount of filler data must be generated towards the TDM interface.

PW frames that are received out of order may be dropped or reordered at the discretion of the egress PE.

Frame loss causes degradation of the perceived audio quality of voice services. For TDM timeslots known to be transporting voice services, the contents of the interpolation frames can therefore be important. In the simplest implementation, predefined constant values may be substituted for the lost TDM voice data, resulting in preservation of TDM timing but rapid deterioration of voice quality. A better alternative replays TDM data, so that each timeslot is fed with data previously received; if the TDM system utilizes CAS signaling then data shall be replayed in such a fashion as to ensure the integrity of CAS signaling. In more sophisticated implementations, each timeslot known to be carrying voice services is analyzed and packet loss concealment techniques are utilized.

6.8 Handling the L, M and R bits

The following procedure shall be used by the egress PE in a given TDMoPSN service:

When $L=0$, $M=00$ is received

The PSN CES IWF shall clear any existing alarm conditions related to these bits.

When $L=1$, $M=00$ is received

The PSN CES IWF shall ignore the payload and generate AIS or Trunk Conditioning on its TDM interface. AIS generation applies to structure-aware trail-extended and structure-agnostic modes. Trunk Conditioning generation applies to the structure-aware trail-terminated mode. The PSN CES IWF should suppress alarms that result from buffer starvation.

When $L=0$, $M=10$ is received

The PSN CES IWF shall generate TDM RAI on its TDM interface. This response applies only to structure-aware trail-extended mode.

For all other combinations of L and M

The PSN CES IWF shall ignore these values and operate as if L=0 and M=00 had been received.

When a transition in R occurs (from 0 to 1)

The PSN CES IWF shall generate the applicable alarm / notification to the NMS.

When a transition in R occurs (from 1 to 0)

The PSN CES IWF shall clear the applicable alarm / notification to the NMS.

6.9 Jitter

In order to compensate for packet delay variation, which exists in any PSN network a jitter buffer, shall be provided. The length of this buffer should be configurable and may be dynamic (i.e. grow and shrink in length according to the statistics of the delay variation).

7. Clock Recovery

TDM networks are inherently synchronous; somewhere in the network there will always be at least one extremely accurate primary reference clock, with long-term accuracy of one part in 10^{11} . This node, whose accuracy is called “Stratum 1”, provides reference timing to secondary nodes with lower “Stratum 2” accuracy, and these in turn provide a reference clock to “Stratum 3” nodes. This hierarchy of time synchronization is essential for the proper functioning of the network as a whole; for details, see [25] or [6]. The use of time standards less accurate than Stratum 3 is not recommended as it may result in service impairments.

Packets in PSN networks reach their destination delayed with a random component, known as jitter. When emulating TDM on a PSN network, it is possible to overcome this randomness by using a “jitter buffer” on all incoming data, assuming the proper time reference is available. The challenge, however, is that the original TDM time reference information may not be disseminated through the PSN network.

In the broadest terms, there are two methods of overcoming this difficulty: in one method, the timing information is provided by some means independent of the PSN network, while in the other, the timing must be transferred over the PSN network.

For example, assume the entire TDM infrastructure (or at least major portions of it) is replaced by a TDMoPSN infrastructure. Timing information shall be delivered over the PSN network, and the reconstructed TDM stream should conform to ITU-T recommendations G.823 [7] for E1 and G.824 [8] for T1 trunks. When it is not practical to provision an accurate local time reference, then clock recovery should be performed based on the rate of arrival of incoming packets by using an appropriate averaging process that negates the effect of zero-mean random jitter. A phase locked loop (PLL) is typically used for this purpose.

The regenerated clock should conform to ITU-T recommendations G.823 [7] for E1 and G.824 [8] for T1 trunks.

However, TDMoPSN is frequently used in a “toll-bypass” scenario, where a PSN connects two existing TDM networks. In such applications, both TDMoPSN devices shall receive accurate timing information from the TDM networks to which they connect and shall use this local timing over the PSN network.

8. PSN CES and ATM CES Service Interworking

Figure 8-1 shows a case where the TDM data is transmitted across an ATM and PSN network. The TDM traffic is carried over the ATM network using AAL1 circuit emulation and is carried over the PSN using TDMoPSN, as defined in this document.

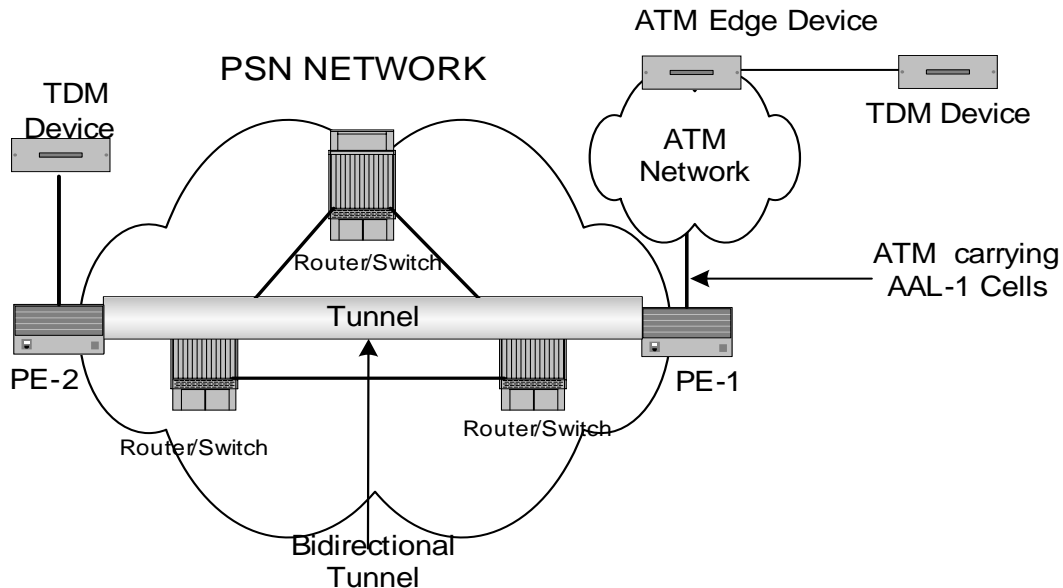


Figure 8-1 ATM-CES Service Interworking with TDMoPSN.

Figure 8-2 shows two possible methods of transporting TDM signals across tandem ATM and PSN networks. One method is to terminate the ATM CES at the interworking point to generate the TDM signals, and then perform TDMoPSN for transporting the TDM stream over the PSN. This method is complex because it involves two stages of circuit emulation (i.e., ATM CES and PSN CES).

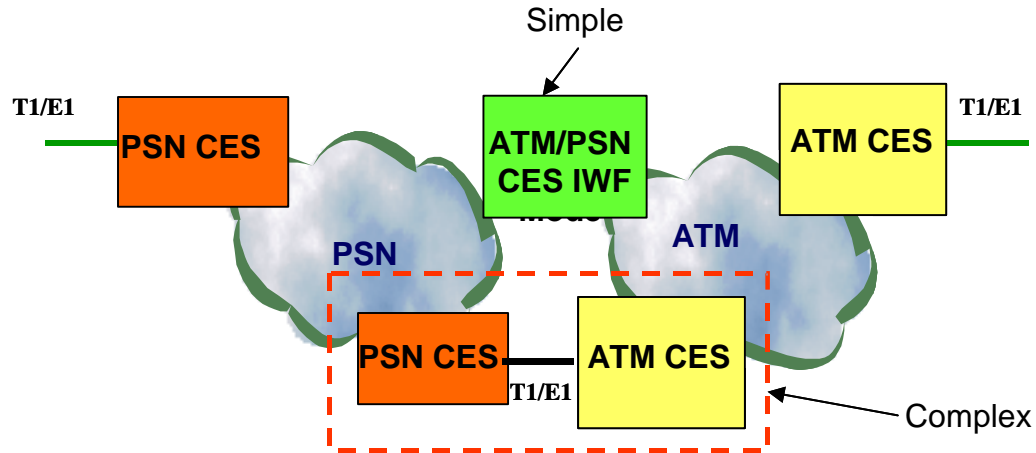


Figure 8-2 Possible methods for ATM-CES and PSN-CES Service Interworking.

A second method is to directly generate TDMoPSN packets from the incoming ATM CES cells and vice versa. This method is only possible if the PSN CES, as proposed in this document, is based on AAL1. Referring to Figure 8-1, PE-1 (ATM/PSN CES IWF) extracts the AAL1 PDUs from the ATM stream, and maps them (according to VCI/VPI) to CBID, appends a TDMoPSN header, and builds a TDMoPSN packet. At the remote side, PE-2 (PSN CES IWF) removes the headers, reassembles the bit stream from the AAL1 PDUs and restores the TDM traffic. This method is simple and is the preferred method. The simplicity of this interworking method can be seen in Figure 8-3.

When AAL1 uses the partial cell fill option as described in af-vtoa-0078.000 [9] Section 2.2.2 and ITU-T Recommendation I.363.1 [11] Section 2.5.2.5, removal of the dummy or fill octets prior to interworking with the PSN to conserve bandwidth in the packet network is for further study.

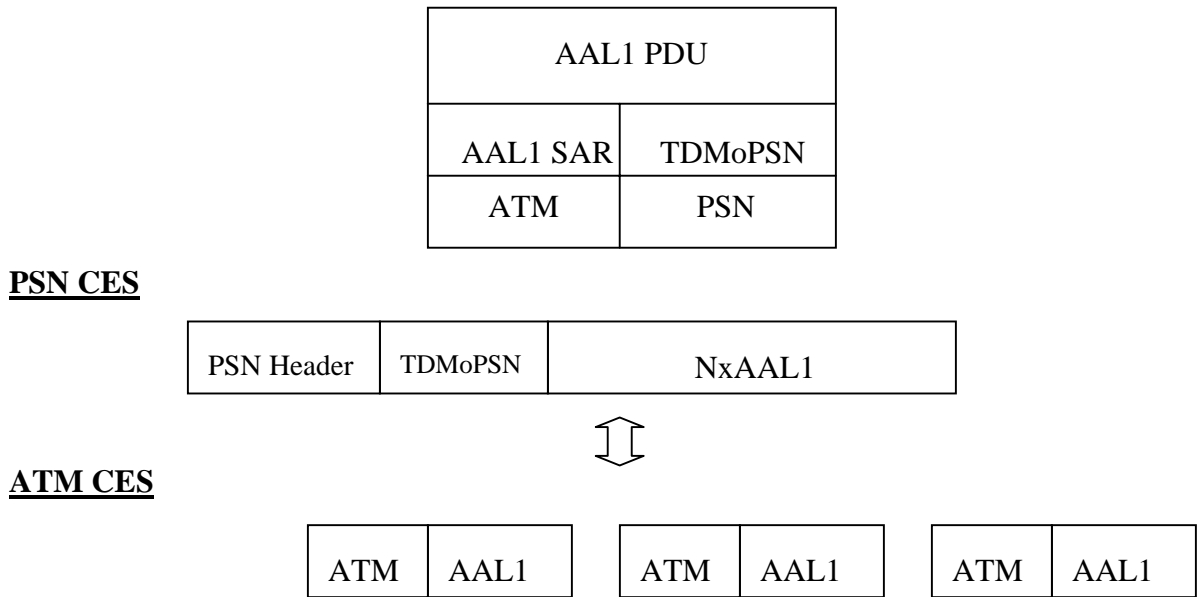


Figure 8-3 Simple interworking between ATM CES and PSN CES.

9. ATM CES and PSN CES Service Interworking Fault Management

This section describes behavior at the ATM CES / PSN CES IWF under various defect conditions. Appendix B.2 contains further details and state diagrams regarding behavior under applicable defect conditions; it is provided for information only.

9.1 Trunk Conditioning for ATM CES to PSN CES Interworking

This section describes the trunk conditioning behavior for the case where an ATM CES and a PSN CES communicate through an IWF. Since ATM-CES does not support structure-aware trail-extended mode, the PSN-CES shall operate in either structure-aware trail-terminated mode or structure-agnostic mode.

9.2 ATM Failure

Structured Emulation: for ATM CES to PSN CES interworking as shown in Figure 9-1, when ATM failure is detected on the ATM interface of the IWF, the IWF stops sending data packets as well as any PW CV or PW PM OAM packets downstream, and instead sends pseudo-wire Forward Defect Indication (PW FDI) downstream. The IWF may optionally generate dummy packets (packets with dummy payload or no payload) and set the flags to L=1, M=00. PW FDI may be conveyed by an in-band OAM packet [12] or an out-of-band signaling message.

In the case of loss of cell (LOC), the IWF also raises the corresponding alarm to the management system.

Upon detection of persistent buffer starvation, the egress PSN CES IWF shall send Trunk Conditioning downstream and optionally upstream. Note that reception of PW FDI or packets with L=1 and M=00 suppresses an alarm from being raised.

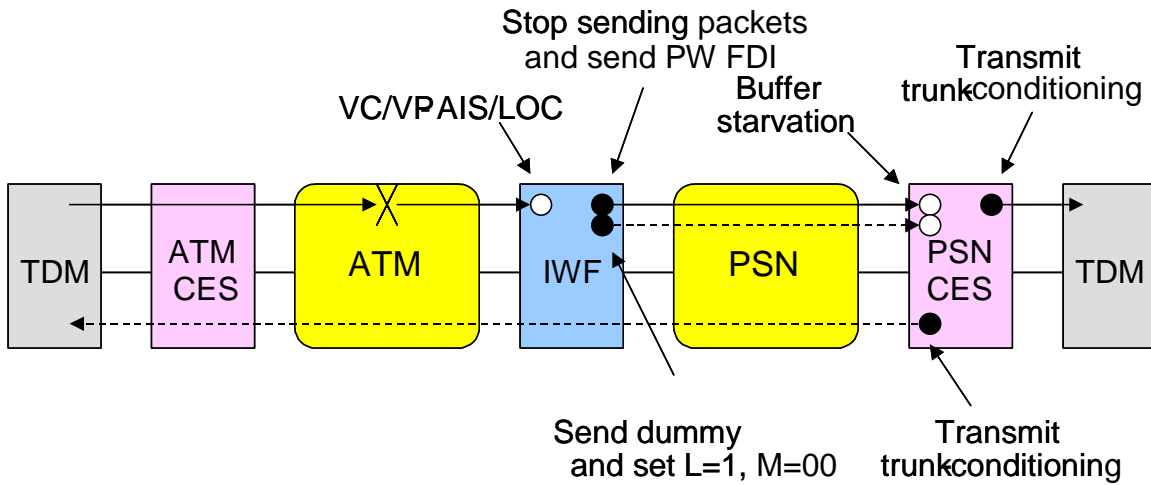


Figure 9-1 ATM CES to PSN CES Trunk Conditioning for ATM Failure (Structure-Aware Trail-Terminated).

Unstructured Emulation: for ATM CES to PSN CES interworking as shown in Figure 9-2, when ATM failure is detected on the ATM interface of the IWF, the IWF stops sending data packets as well as any PW CV or PW PM OAM packets downstream, and sends PW FDI downstream instead. Alternatively, the IWF may generate dummy packets (packets with a dummy payload or no payload) and set the flags to L=1, M=00. Upon detection of persistent buffer starvation, the egress PSN CES IWF shall send AIS downstream. Note that reception of PW FDI or packets with L=1 and M=00 suppresses an alarm from being raised.

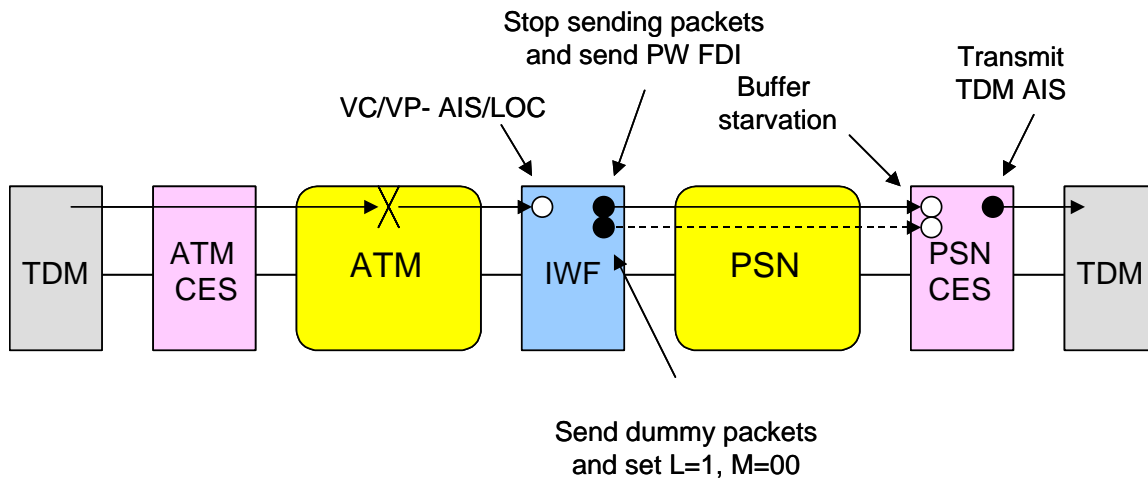


Figure 9-2 ATM CES to PSN CES Trunk Conditioning for ATM Failure (Unstructured).

Rule 14: Upon detection of ATM failure in both structured and unstructured circuit emulation, the ATM CES to PSN CES IWF should stop sending data packets as well as PW CV and PW PM OAM packets downstream and send PW FDI downstream instead. Alternatively, it may send dummy packets with L=1 and M=00 in the downstream direction. If the defect is due to LOC, the IWF shall also raise the corresponding alarm. This is shown in Figure 9-1 and Figure 9-2.

9.3 PSN Packet Loss

Structured Emulation: for ATM CES to PSN CES interworking as shown in Figure 9-3, when packet loss or PSN AIS is detected on the PSN interface of the IWF, the IWF generates ATM AIS and stops sending other types of cells (including CC and PM). It also optionally sets the R bit in the upstream direction. Upon reception of ATM AIS, the egress ATM CES IWF generates trunk conditioning in both downstream and upstream directions.

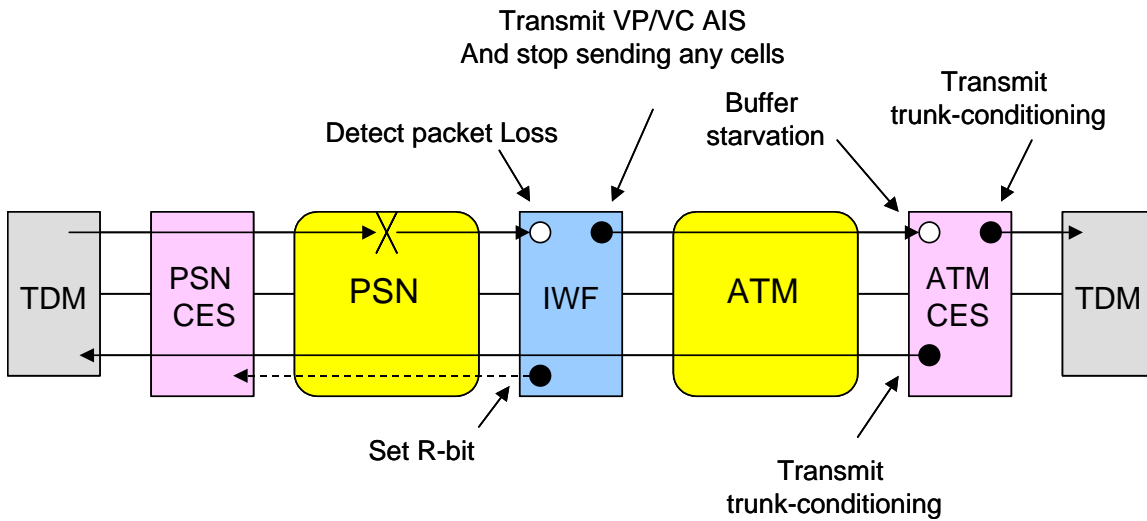


Figure 9-3 ATM CES to PSN CES Trunk Conditioning for AIS/LOP (Structured).

Unstructured Emulation: for ATM CES to PSN CES interworking as shown in Figure 9-4, when packet loss or PSN AIS is detected at the PSN interface of the IWF, the IWF generates ATM AIS and stops sending other types of cells (including CC and PM). It also optionally sets the R bit to 1 in the upstream direction. Upon reception of ATM AIS, the egress ATM CES IWF generates TDM AIS in the downstream direction.

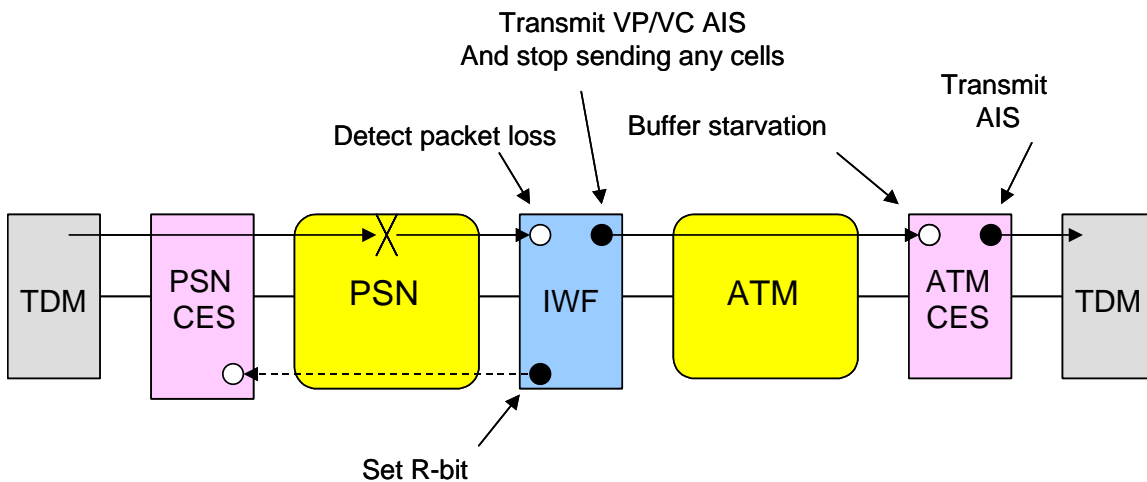


Figure 9-4 ATM CES to PSN CES Trunk Conditioning for AIS/LOP (Unstructured).

Rule 15: Upon detection of packet loss in both structured and unstructured circuit emulation, the PSN CES to ATM CES IWF should set the R-bit to 1 in the upstream direction. It shall also generate VP/VC AIS downstream, and shall stop sending any other cells (e.g., CC, PM, etc.). If the defect is due to loss of packet, the IWF shall also raise the appropriate alarm. This behavior is shown in Figure 9-3 and Figure 9-4.

Rule 16: For unstructured service, all alarms received at the input of the ATM/PSN CES interworking function are carried through to the output service interface without modification. This includes any input at the ATM and PSN interfaces.

10. ATM to TDM via PSN (PE-1 to PE-2) Frame Processing

10.1 TDMoPSN Frame Processing at PE-1

10.1.1 Generating TDMoPSN Frames at the ATM CES / PSN CES Interface PE (PE-1)

TDMoPSN frames are generated from an ATM interface by aggregating several cell payloads into one packet, and then adding control, multiplexing and PSN headers.

10.1.2 Generating the TDMoPSN Payload

AAL1 cell headers are removed, and the 48-octet payloads are concatenated to form one packet. The number of cells per packet is as configured.

10.1.3 Generating the TDMoPSN Control Word

10.1.3.1 Setting the Sequence Number

See Section 6.3.1.

10.1.3.2 Generating the L, M and R bits

The following procedure shall be used by the ATM/PSN -CES IWF (PE-1):

The PSN CES to ATM CES IWF, when configured to do so, should set the flags of the PSN CES header as follows:

Set L=1, M=00

When an ATM or physical layer failure is detected at the ATM interface of the PSN/ATM CES IWF. Packets with the L=1 and M=00 will usually contain the control word only; these packets should be sent periodically. However, if data cells (AAL1 cells) are received from the ATM network, the IWF should set the L bit to 1 in packets containing those AAL1 cells. When the ATM defect state clears, the IWF shall send packets with the L and M bits cleared to 0 and 00 respectively.

Set L=0, M=00

When no ATM or physical layer failure is detected at the ATM interface of the PSN/ATM CES IWF.

Other combinations of L and M are reserved for future use.

Set R = 1 or 0

See Section 6.3.2.

10.1.3.3 Setting the Length Field

See Section 6.3.3.

10.1.4 Generating the Multiplexing Header

See Section 6.4.

10.1.5 Generating the Optional RTP Header

See Section 6.5.

10.1.6 Generating the PSN Header

See Section 6.6.

10.2 Receiving TDMoPSN Frames at the PSN-CES IWF (PE-2)

As defined in Section 6.7.

10.2.1 Defect Handling

See Section 6.8.

10.2.2 OAM Cell Handling

ATM OAM cells are terminated locally at the PE1 ATM interface and are not transmitted onto the PSN CES. The fault states must be mapped to the corresponding PSN states according to Section 9.2.

10.3 TDM to ATM via PSN (PE-2 to PE-1) Frame Processing

10.3.1 TDMoPSN Frame Processing at PE-2

10.3.1.1 Generating TDMoPSN Frames at the PSN-CES IWF (PE-2)

As defined in Section 6.1.

10.3.2 TDMoPSN Frame Processing at PE-1

10.3.2.1 Receiving TDMoPSN Frames at the ATM CES / TDM CES IWF (PE-1)

Upon receiving a TDMoPSN frame, PE-1 checks the layer 2 checksum. If the checksum is incorrect, the frame is discarded. Otherwise, it processes the TDMoPSN frame header fields. PE-1 performs the following actions (not necessarily in the order shown):

- PE-1 processes the length and sequence number fields.
- The sequence number field is calculated as in Section 6.3.1.
- If the PDU has the correct sequence number, then it can be inserted into the play-out buffer.
- PDUs that are received out of order may be dropped or reordered at the discretion of the egress PE.
- AAL-1 cells are extracted from the PSN frame PDU and ATM cells are generated as follows:
 - The Circuit Bundle ID is mapped to the VC/VP fields as configured.
 - The PTI field value is set to 000 as specified in [9].
 - The C bit is set to 0 as specified in [9].
- The CRC, P and SN bits of the sub-frames are not checked.

10.3.2.2 Defect Handling

Refer to Section 5.

10.3.2.3 OAM Cell Handling

OAM cell mapping is not applicable.

11. Glossary

AAL	ATM Adaptation Layer
AIS	Alarm Indication Signal
ATM-AIS	VP/VC-AIS (F4/F5 AIS)
ATM Failure	LOC or F3/F4/F5 AIS
CB	Circuit Bundle
CBID	Circuit Bundle ID
CC	Connectivity Check (pertaining to ATM)
CES	Circuit Emulation Service
CV	Connectivity Verification pertaining to a PW
D/S	Down Stream (continuing in the same direction as the defect that is detected by the IWF)
FDI	Forward Defect Identifier pertaining to a PW
IWF	InterWorking Function
LOF	Loss of Frame
LOS	Loss of Signal
LSP	Label Switched Path
NMS	Network Management System
OAM	Operation, Administration, Maintenance
OOF	Out of Frame synchronization
PDI	Payload Defect Indicator
PE	Provider Edge
PHB	Per Hop Behavior
PL	Payload
PSN	Packet Switched Network
PSN CES	PSN Circuit Emulation Service. Equivalent to TDMoPSN
PW	Pseudo Wire
RAI	TDM Reverse Alarm Indication
RDI	Remote Defect Indicator
RTP	Real Time Protocol

TC Trunk Conditioning (based on Bellcore TR-NWT-000170)
TDMoPSN TDM over PSN. Equivalent to PSN CES.
U/S Up Stream (reverse direction to the defect detected by the IWF)

12. References

- [1] ITU-T Recommendation G.702 (1988) - Digital Hierarchy Bit Rates.
- [2] ANSI T1.107 (1995): Digital Hierarchy - Format Specification.
- [3] ITU-T Recommendation G.703 (1998): Physical / Electrical Characteristics of Hierarchical Digital Interfaces.
- [4] ITU-T Recommendation G.704 (1998): Synchronous Frame Structures Used at 1544, 6312, 2048, 8448 and 44736 Kbit/s Hierarchical Levels.
- [5] ITU-T Recommendation G.751 (1988): Digital Multiplex Equipment Operating at the third order bit rate of 34368 Kbit/s and the fourth order bit rate of 139264 Kbit/s and Using Positive Justification.
- [6] ITU-T Recommendation G.810 (1996): Definitions and Terminology for Synchronization Networks.
- [7] ITU-T Recommendation G.823 (2000): The Control of Jitter and Wander within Digital Networks which are based on the 2048 Kbit/s Hierarchy.
- [8] ITU-T Recommendation G.824 (2000): The Control of Jitter and Wander within Digital Networks which are based on the 1544 Kbit/s Hierarchy.
- [9] ATM Forum af-vtoa-0078.000 (1997) Circuit Emulation Service (CES) 2.0.
- [10] IETF RFC 3550 (2003): RTP: A Transport Protocol for Real-Time Applications.
- [11] ITU-T Recommendation I.363.1 (1996) B-ISDN ATM Adaptation Layer Specification: Type 1 AAL.
- [12] ITU-T Recommendation Y.1711(2002) "OAM Mechanisms for MPLS Networks".
- [13] ITU-T Recommendation I.610 (1999) "B-ISDN Operation and Maintenance Principles and Functions".
- [14] Lau, J., et al, "Layer Two Tunneling Protocol version 3" , internet draft <draft-ietf-l2tpext-l2tp-base-11.txt>, October 2003.
- [15] Kompella, K., et al, "Detecting MPLS Data Plane Failure" , Internet Draft <draft-ietf-mpls-lsp-ping-04.txt>, October 2003.
- [16] Nadeau, T., "Pseudo Wire Virtual Circuit Connection Verification (VCCV)", Internet Draft <draft-ietf-pwe3-vccv-02.txt>, October 2003.
- [17] Katz, D., Ward, D., "Bidirectional Forwarding Detection", Internet Draft <draft-katz-word-bfd-01.txt>, August 2003.
- [18] Nadeau, T., "Pseudo Wire (PW) OAM Message Mapping", Internet Draft <draft-nadeau-oam-msg-map-04.txt>, October 2003.

- [19] Martini, L., Rosen, E., Smith, T., “Pseudo Wire Setup and Maintenance Using LDP”, Internet Draft <draft-ietf-pwe3-control-protocol-05.txt>, December 2003.
- [20] Martini, L. , Rosen, E., Smith, T., “RSVP-TE Extensions to RSVP for LSP Tunnels”, RFC 3209.
- [21] Aissaoui, M., et al, “OAM Procedure for VPWS Interworking”, Internet Draft <draft-aissoui-l2vpn-vpws-iw-oam-00.txt>, August 2003.
- [22] ITU-T Recommendation Y.1712 (2002) “OAM Functionality for ATM-MPLS Interworking”.
- [23] Postel, J. "Internet Control Message Protocol", RFC 792.
- [24] Bellcore TR-NWT-000170 Issue 2.
- [25] ANSI/T1.101-1999 “Synchronization Interface Standard”.
- [26] ITU-T Recommendation I.231.1 (1998) “Circuit Mode Bearer Service Categories – Circuit Mode 64 kbit/s Unrestricted, 8 kHz Structured Bearer Service.
- [27] ITU-T Recommendation Y.1413 (2004) “TDM MPLS Network Interworking – User Plane Interworking”.

A. PW Fault Detection

This appendix describes some methods for detecting the PW status in various PSN configurations.

A.1 PW Down Condition

A PW is declared Down if any of the following conditions are met:

1. The PE receives a remote PW or PSN Tunnel status message [19] that indicates that one or both directions of the PW or PSN Tunnel are down.
2. The PE receives an inband PW or PSN OAM message that indicates that one or both directions of the PW are down (e.g., BFD [17], LSP-Ping [15], VCCV [16], Y.1711 [12] CV, FDI or BDI).

A.1.1 MPLS Tunnel Down Conditions

The MPLS Tunnel (LSP) status is declared Down if any of the following conditions are met:

1. A physical layer alarm is detected on the MPLS interface.
2. An MPLS-specific OAM mechanism, such as LSP-Ping [15], BFD [17], or Y.1711 [12] CV or FDI/BDI or the Hello protocol (used when RSVP-TE [20] is used to set up the tunnel), indicates that the MPLS tunnel is Down.

A.1.2 L2TPv3 Tunnel Down Conditions [14]

The L2TPv3 Tunnel status is declared Down if any of the following conditions are met:

1. A physical layer alarm is detected on the IP interface.
2. A specific OAM mechanism, such as ICMP-Ping [23], BFD [17], or an L2TPv3 Keep Alive message (fault notification via SCCN and CDN messages), indicates that the L2TP tunnel is Down.

A.1.3 UDP / IP Tunnel Down Conditions

The UDP/IP Tunnel status is declared Down if any of the following conditions are met:

1. A physical layer alarm is detected on the IP interface.
2. A specific OAM mechanism, such as ICMP-Ping [23] or BFD [17], indicates that the UDP/IP Tunnel is Down.

A.1.4 Ethernet Tunnel Down Conditions

1. A physical layer alarm is detected on the Ethernet interface (e.g., via 802.3ah OAM).

2. An Ethernet OAM mechanism, such as ETH-CC or ETH-AIS (ITU-T Y.ethoam), indicates an Ethernet layer defect.

A.2 PW Up Condition

When the PE determines that all previously existing failures have disappeared, it should send a message to its peer to indicate a PW UP condition.

B. Defect Conditions and Defect-Handling State Diagrams

B.1 PSN-CES IWF Defect Handling

This section discusses the behavior of the PSN-CES IWF in response to defect conditions. It outlines all possible defect conditions and the corresponding defect state diagram for the PSN-CES IWF.

B.1.1 PSN-CES IWF Defect Conditions

Figure B-1 shows all relevant defects that could happen when running circuit emulation over a PSN network.

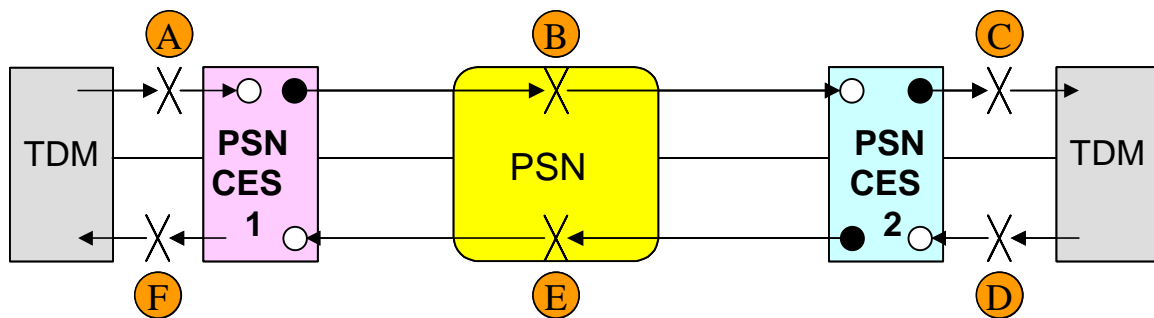


Figure B-1 Defect Conditions related to Circuit Emulation over PSN.

Note: PSN CES 1 and PSN CES 2 indicate PSN-CES IWFs.

To simplify this description, only the behavior of PSN-CES IWF 1 is considered in the following sections. The behavior of PSN-CES IWF 2 is similar to PSN-CES IWF 1.

From a defect handling perspective, an implementation of circuit emulation over PSN could fall into one of three categories:

- Structure-agnostic mode (Unstructured circuit emulation)
- Structure-aware trail-terminated mode (Structured circuit emulation of T1/E1)
- Structure-aware trail-extended mode (Structured circuit emulation of NxDS0).

B.1.2 PSN-CES IWF Defect States (Structure-agnostic mode)

Figure B-2 shows the state diagram of the PSN-CES IWF 1 in relation to defects identified in Figure B-1, assuming the PSN-CES IWFs are running unstructured circuit emulation.

For simplicity, only single failure conditions are considered in this section. In general, multiple failure conditions could force the PSN-CES IWF to be in multiple states at the same time.

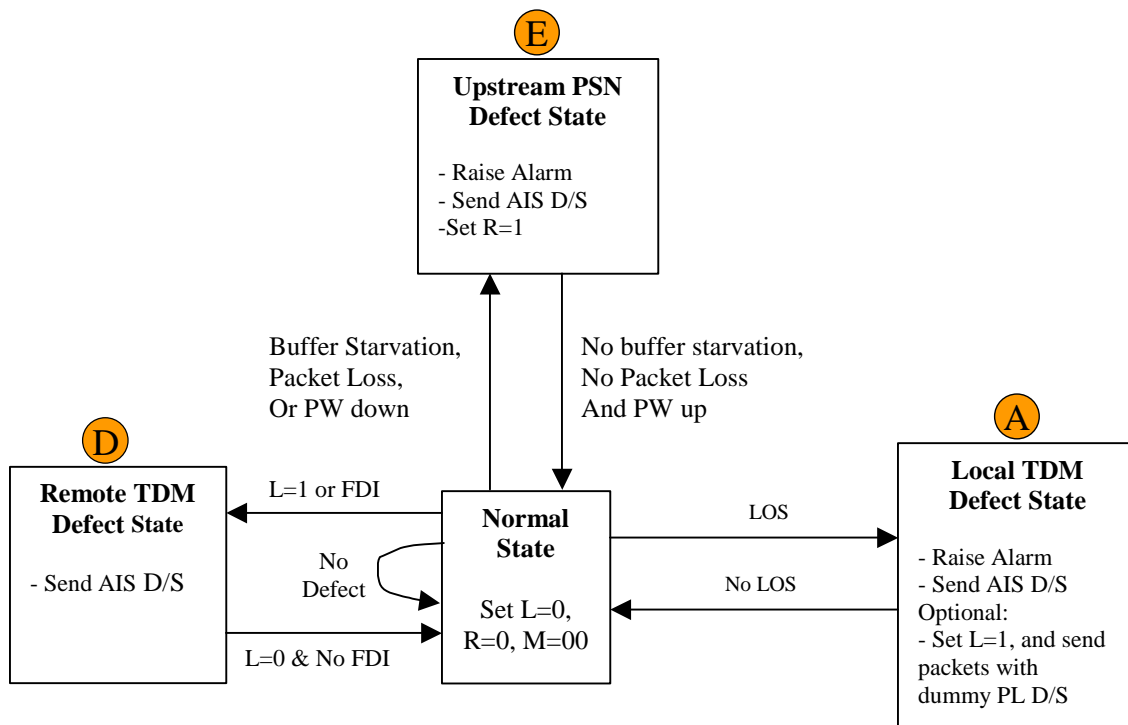


Figure B-2 PSN-CES IWF State Diagram (Structure-Agnostic).

When no defect is detected in the PSN or TDM network, the PSN-CES IWF 1 is in the Normal state. In the Normal State, the PSN-CES IWF 1 receives and transmits packets, in which the flags are clear (L=0, M=00, R=0).

When Loss of Signal (LOS) at the TDM port (event A) is detected, the PSN-CES IWF 1 enters the Local TDM defect state. In this state, it should raise the appropriate alarm and send unframed AIS (all 1's) downstream. It may optionally send dummy packets with L=1 and M=00.

When the PSN-CES IWF 1 detects packet loss, or a down PW or buffer starvation at the PSN interface, it should raise the corresponding alarm and send unframed AIS (all 1's) downstream. It should also set R=1 in the reverse direction.

If the PSN-CES IWF receives packets with L=1 and M=00, or PSN or PW FDI, it should send AIS downstream and not raise any alarm.

B.1.3 PSN-CES IWF Defect States (Structure-aware trail-extended mode)

Figure B-3 shows the state diagram of the PSN-CES IWF 1 related to defects identified in Figure B-1, assuming the PSN-CES IWFs are doing structured circuit emulation of T1/E1.

For simplicity, only single failure conditions are considered in this section. In general, multiple failure conditions could force the PSN-CES IWF 1 into multiple states at the same time.

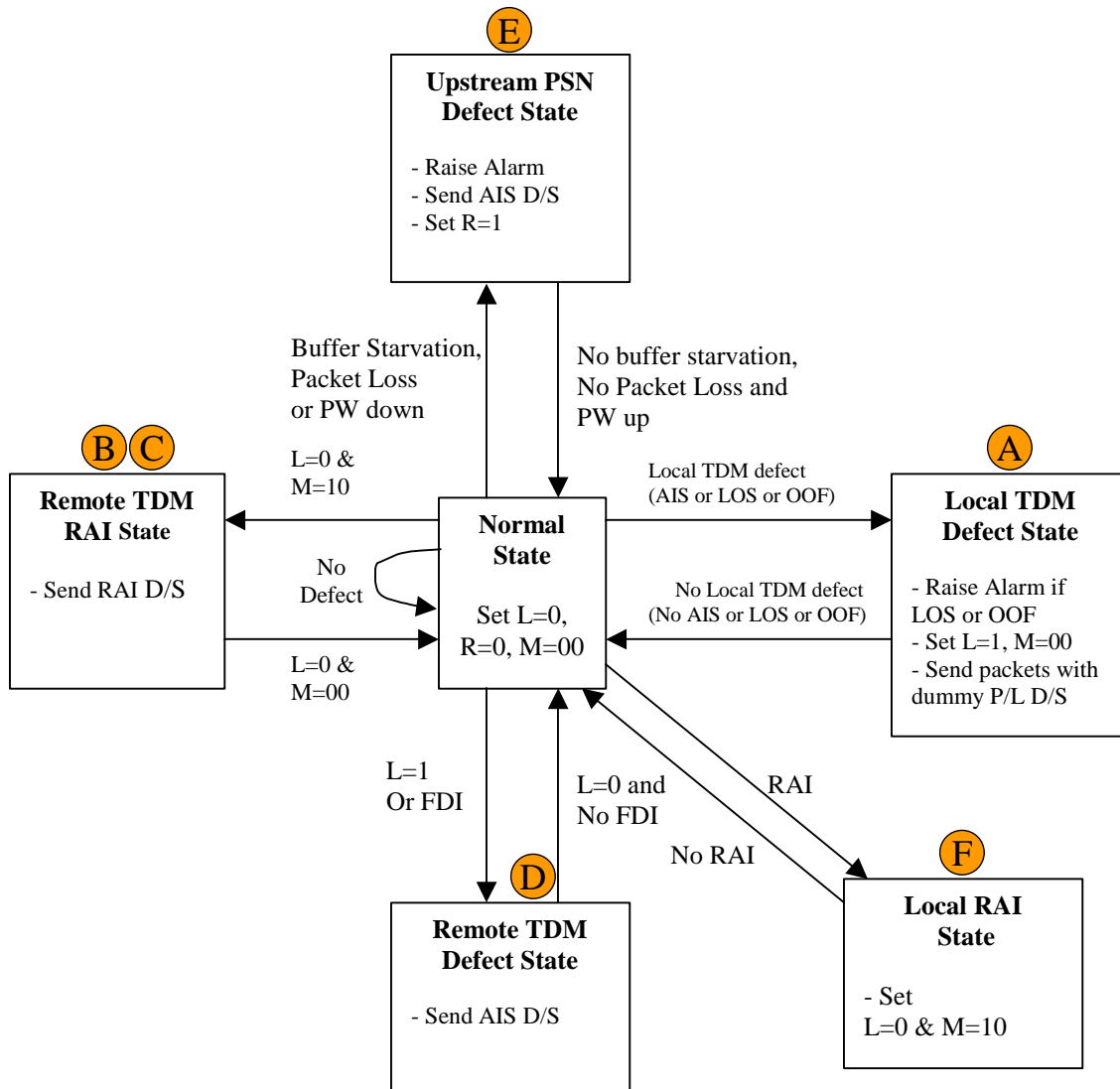


Figure B-3 PSN-CES IWF State Diagram (Structure-Aware Trail-Extended).

When no defect is detected in the PSN or TDM network, the PSN-CES IWF 1 is in the Normal state. In the Normal State, the PSN-CES IWF 1 receives and transmits packets in which the flags are clear ($L=0$, $M=00$, $R=0$).

If LOS, OOF, or TDM AIS at the TDM port (event A) is detected, the PSN-CES IWF 1 enters the Local TDM Defect state. In the case of LOS or OOF, the corresponding alarm should be raised. Since structured circuit emulation cannot directly transport TDM AIS signals downstream, the PSN-CES IWF 1 should set the L-bit to 1 and send dummy packets downstream.

Upon reception of PSN or PW FDI or dummy packets with $L=1$, the downstream PSN-CES IWF 2, generates unframed AIS (all 1's) downstream.

If the PSN-CES IWF 1 detects packet loss, or Pseudo wire being down or buffer starvation at the PSN interface, it should raise the corresponding alarm and send unframed AIS (all 1's) downstream. It should also set R to 1 in the reverse direction.

If TDM RAI is detected at the TDM interface, the PSN-CES IWF 1 should set L to 0 and M to 10. This is required since structured circuit emulation cannot directly transport RAI downstream. When these packets with L=0 and M=10 are detected, the downstream PSN-CES IWF should send RAI downstream.

B.1.4 PSN-CES IWF Defect States (Structure-aware trail-Terminated mode)

Figure B-4 shows the state diagram of the PSN-CES IWF 1 related to defects identified in Figure 4-1, assuming the PSN-CES IWFs are doing NxDS0 structured circuit emulation.

For simplicity, only single failure conditions are considered in this section. In general, multiple failure conditions could force the PSN-CES IWF 1 into multiple states at the same time.

When there is no defect detected in the PSN or TDM network, the PSN-CES IWF 1 is in the Normal state. In the Normal State, the PSN-CES IWF 1 receives and transmits packets with the flags cleared (L=0, M=00, R=0).

If the PSN-CES IWF 1 detects LOS, OOF, or TDM AIS at its TDM port (event A), it enters the Local TDM Defect state. In case of LOS or OOF, the corresponding alarm should be raised. The PSN-CES IWF 1 should also send Trunk Conditioning (according to [24]) downstream while transmitting RAI upstream. It may optionally send dummy packets with L=1 and M=00.

If the PSN-CES IWF 1 detects packet loss, or a down PW or buffer starvation at the PSN interface, it should raise the corresponding alarm and send Trunk Conditioning upstream and downstream. It should also set R to 1 in the reverse direction.

If TDM RAI is detected at the TDM interface, the PSN-CES IWF 1 should terminate it.

When the PSN-CES IWF 1 receives packets with L=1, it should send Trunk Conditioning downstream.

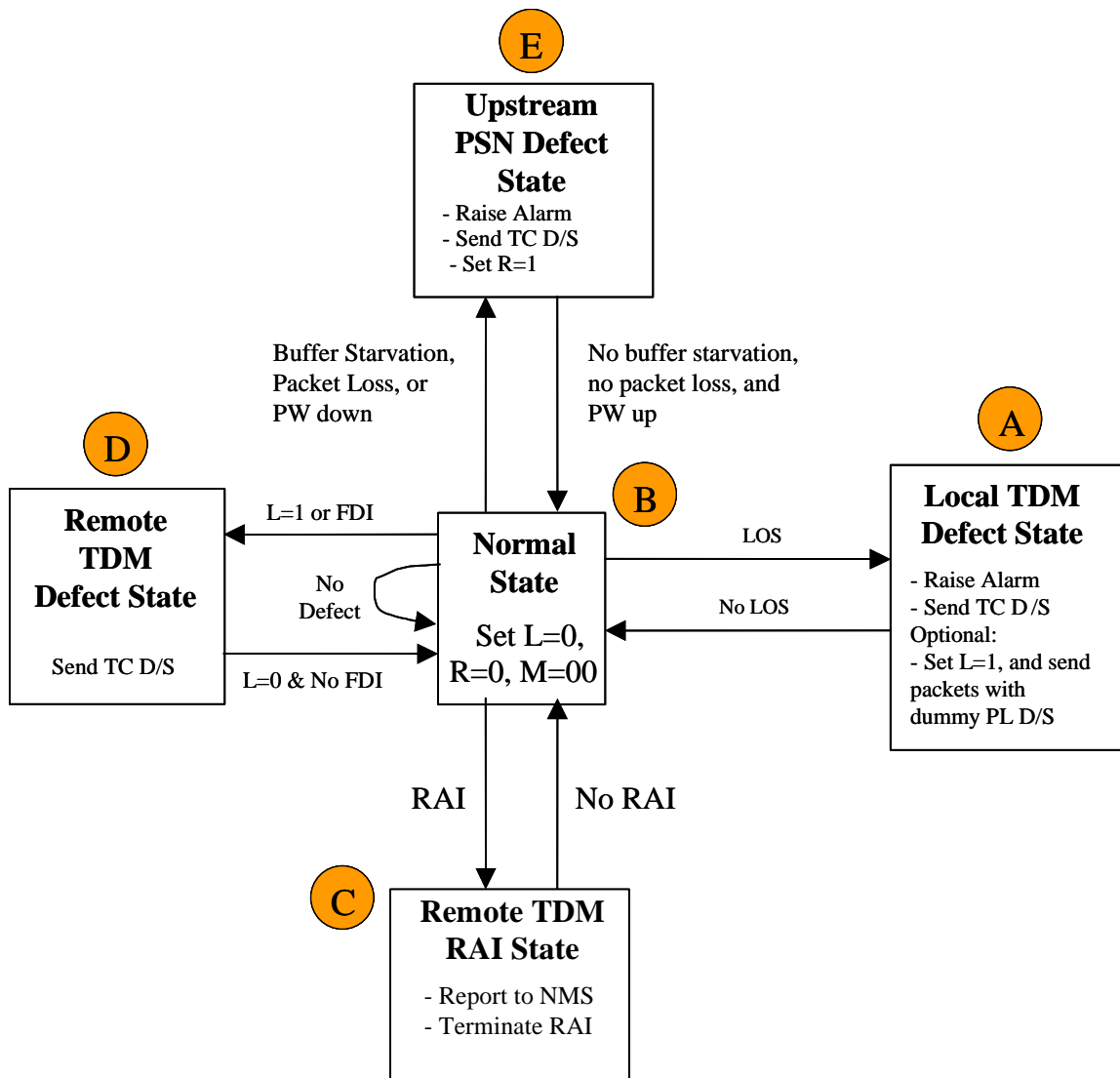


Figure B-4 PSN-CES IWF State Diagram (Structure-Aware Trail-Terminated).

B.2 PSN/ATM-CES IWF Defect Handling

This section discusses the behavior of the PSN-CES/ATM-CES IWF in response to defect conditions. It outlines all relevant defects conditions and the corresponding defect state diagram for the PSN/ATM-CES IWF.

B.2.1 PSN-CES IWF Defect Conditions

Figure B-5 shows all relevant defects that could happen when interworking the PSN CES and ATM CES.

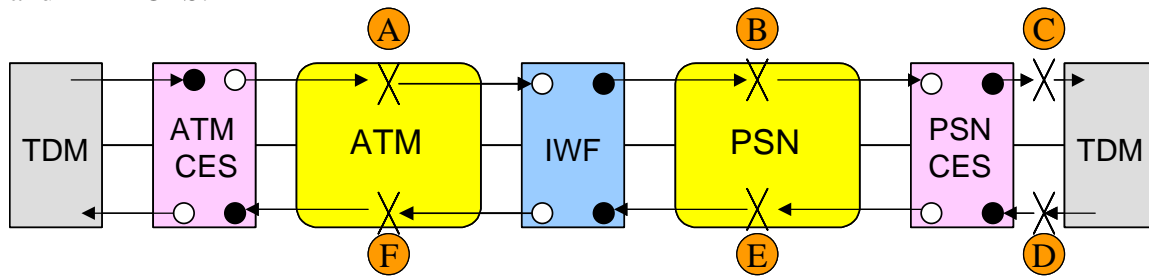


Figure B-5 Defect Conditions related to interworking of PSN/ATM-CES.

Note: IWF indicates a PSN/ATM-CES IWF. ATM CES indicates an ATM-CES IWF, and PSN CES indicates a PSN-CES IWF.

To simplify this description, only the behavior of the PSN/ATM-CES IWF is considered in the following sections. The behavior of the PSN-CES IWF is explained in previous sections, and the behavior of the ATM-CES IWF is described in the ATM Forum CES 2.0 specification.

From a defect handling perspective, the PSN-CES and ATM-CES can only be interworked in one of the following methods:

- Structure-Agnostic mode
- Structure-Aware Trail-Terminated mode

B.2.2 PSN/ATM-CES IWF Defect States (Structure-Aware Trail-Terminated)

Figure B-6 shows the state diagram of the PSN/ATM-CES IWF in relation to defects identified in Figure B-5, assuming the PSN/ATM CES IWF is doing structured NxDS0 emulation.

For simplicity, only single failure conditions are considered in this section. In general, multiple failure conditions could cause the PSN/ATM-CES IWF to be in multiple states at the same time.

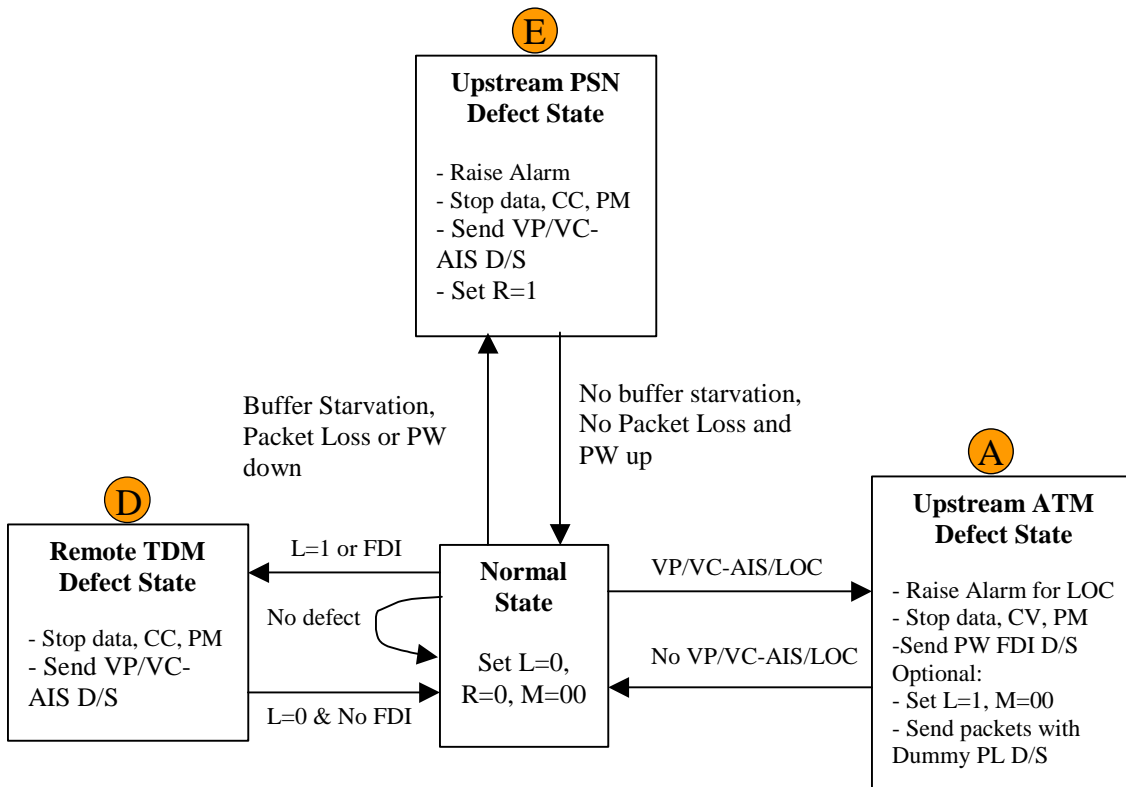


Figure B-6 PSN/ATM-CES IWF State Diagram (Structure-Aware Trail-Terminated).

When no defect is detected in the PSN or TDM network, the PSN/ATM-CES IWF is in the Normal state. In the Normal state, the PSN/ATM-CES IWF receives and transmits packets with the flags cleared (L=0, M=00, R=0).

If the PSN/ATM-CES IWF detects ATM AIS (VP/VC-AIS) or cell loss at its ATM interface (event A), it enters the Local ATM Defect state. In case of LOC, the appropriate alarm should be raised. It should send PW FDI downstream or send dummy packets with L set to 1. In either case, the egress PSN IWF generates Trunk Conditioning toward the TDM network.

If the PSN/ATM –CES IWF detects packet loss, or a down PW or buffer starvation at its PSN interface, it should raise the corresponding alarm. It should also set the R bit to 1 in the reverse direction. To simplify the PSN/ATM-CES IWF as much as possible, Trunk Conditioning is not generated. The IWF sends instead VP/VC-AIS and stops sending data, CC and OAM cells downstream. This will trigger generation of Trunk Conditioning without raising any alarm at the downstream ATM-CES IWF.

If the IWF receives PSN FDI or PW FDI or packets with L=1 and M=00, it should stop sending data, CC and PM OAM cells and send VP/VC AIS instead. This will force the generation of Trunk Conditioning without raising any alarm at the downstream ATM-CES IWF.

B.2.3 PSN/ATM-CES IWF Defect States (Structure-Agnostic)

Figure B-7 shows the state diagram of the PSN/ATM-CES IWF, in relation to defects identified in Figure B-5, assuming the PSN/ATM CES IWF is implementing unstructured circuit emulation. The behavior of the IWF is very similar to the behavior for structure-aware trail-terminated mode.

For simplicity, only single failure conditions are considered in this section. In general, multiple failure conditions could force the PSN/ATM-CES IWF into multiple states at the same time.

When no defect is detected in the PSN or TDM network, the PSN/ATM –CES IWF is in the Normal state. In this state, the PSN/ATM –CES IWF receives and transmits packets with the flags cleared (L=0, M=00, R=0).

If the PSN/ATM –CES IWF detects ATM AIS (VP/VC-AIS) or cell loss at its ATM interface (event A), it enters the Local ATM Defect state. In the case of LOC, the corresponding alarm should be raised. In this state, it should send PW FDI downstream or send dummy packets with the L bit set to 1. In either case, the egress PSN IWF generates TDM AIS towards the TDM network.

If the PSN/ATM –CES IWF detects packet loss, or a down PW or buffer starvation at its PSN interface, it should raise the corresponding alarm. It should also set the R bit to 1 in the reverse direction. To simplify its implementation as much as possible, the IWF does not generate Trunk Conditioning. It sends instead VP/VC-AIS and stops sending data, CC and PM OAM cells downstream. This will trigger TDM AIS without raising any alarm at the downstream ATM-CES IWF.

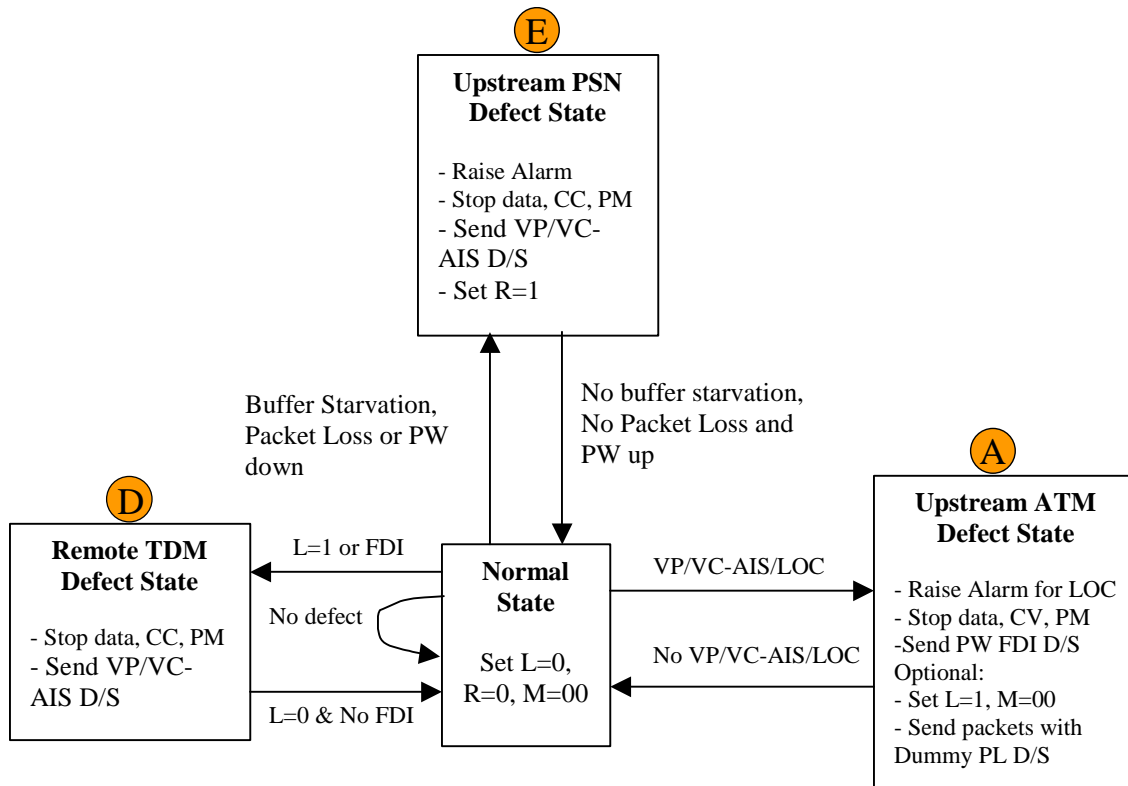


Figure B-7 PSN/ATM-CES IWF State Diagram (Structure-Agnostic).

C. Circuit Emulation over PSN Interworking Modes

This appendix describes the following three modes of operation that apply to circuit emulation over PSN:

- Structure-Agnostic mode
- Structure-aware trail-terminated mode
- Structure-aware trail-extended mode.

The Structure-Agnostic mode is similar to AAL1 Unstructured emulation. The Structure-Aware Trail-Terminated mode is similar to AAL1 Structured emulation. There is no equivalence to AAL1 emulation for the Structure-Aware Trail-extended mode.

C.1 Structure-Agnostic Mode

Figure C-1 depicts the structure-agnostic mode, wherein the TDM stream is transferred without requiring the PSN layer to know its underlying structure. From an OAM perspective, the TDM trail (data + OAM) is transparently transported across the PSN, which provides a single link connection for the TDM client. The TDM trail termination functions are located at the TDM end systems.

Since the TDM circuits are treated as unstructured, all T1/E1 defects indicated in the TDM structure overhead are transparently carried end to end. While there may be no connection between the PSN and TDM domain OAM entities, the TDM monitoring and defect indications are guaranteed to function properly.

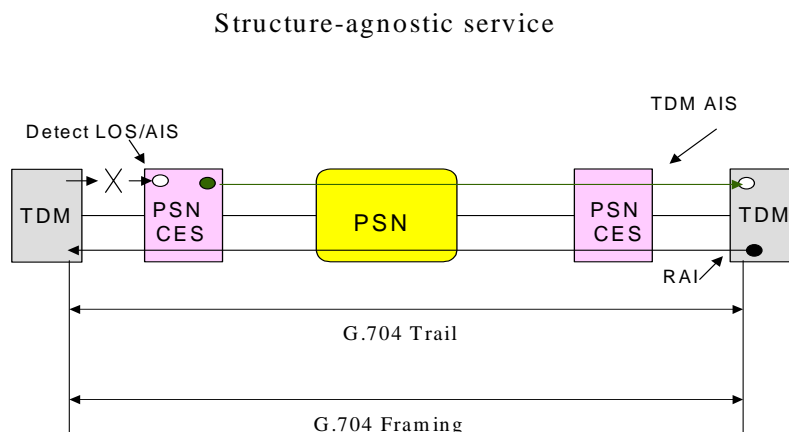


Figure C-1 Structure-Agnostic Mode

C.2 Structure-Aware Trail-Terminated Mode

Figure C-2 depicts the structure-aware trail-terminated mode, wherein the TDM structure overhead is stripped off and terminated prior to transport over the PSN layer. In this case, the TDM trail is NOT extended across the PSN (e.g., TDM AIS or RAI is not transported). The PSN CES IWF becomes the trail termination function, resulting in three separate networks: two TDM networks and a PSN over which the data portion of a basic N*DS0 service is transported. Each network maintains its own OAM functionality.

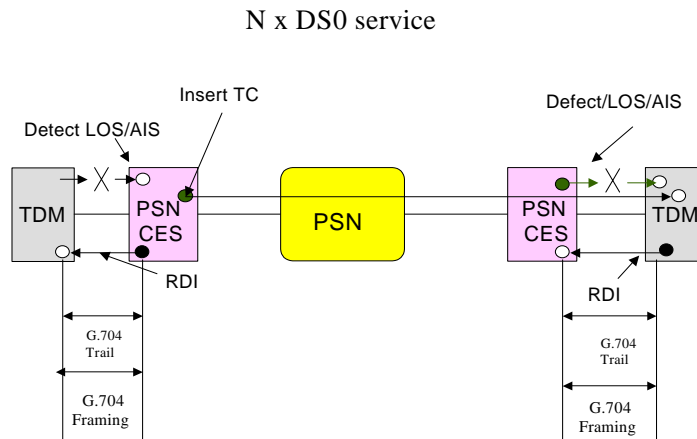


Figure C-2 Structure-Aware Trail-Terminated Mode

A unidirectional break within the TDM network causes TDM AIS to be generated towards the PSN CES IWF. A unidirectional break in the last link feeding into the IWF causes the IWF to detect LOS. In both cases, the IWF (containing the trail termination function) generates TDM RAI back towards the originating TDM end system. It also sends Trunk Conditioning towards the PSN to indicate invalid TDM data. The far-end PSN CES IWF will forward the received trunk conditioning to the destination TDM end system.

C.3 Structure-Aware Trail-Extended Mode

Figure C-3 depicts the structure-aware trail-extended mode, wherein the TDM trail is extended over the PSN as follows. The TDM defect indications are stripped by the PSN CES IWF, as is done in the trail-terminated mode, but their semantics are translated into a different format by means of the L, M and R fields in the PSN packet overhead. The PSN provides a link connection for the TDM client data. The TDM systems at either end of the network are the TDM trail termination points, just as in the structure-agnostic mode.

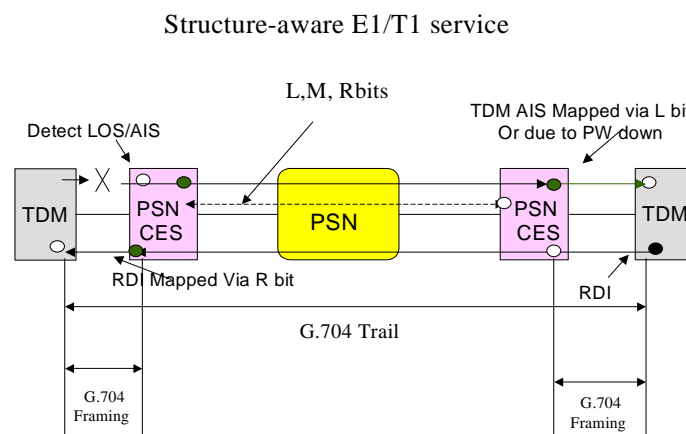


Figure C-3 Structure-Aware Trail-Extended Mode

Since the PSN CES IWF strips off the structure overhead, all defect indications (and error monitoring) must be mapped end-to-end via the L, M and R bits in the control word. This mode is supported only in PSN CES network interworking, but does not apply to service interworking between ATM-CES and PSN-CES, because it is not supported in ATM CES.

C.4 ATM-CES / PSN-CES Service Interworking Modes

For service interworking between an ATM CES and a PSN CES network, two configurations are allowed:

- ATM-CES operating in unstructured mode and PSN CES operating in structure-agnostic mode.

- ATM-CES operating in structured AAL1 mode and PSN-CES operating in structure-aware trail-terminated mode.

The structure-aware trail-extended PSN mode cannot be used for ATM/PSN CES service interworking since there is no corresponding mode in an ATM CES.